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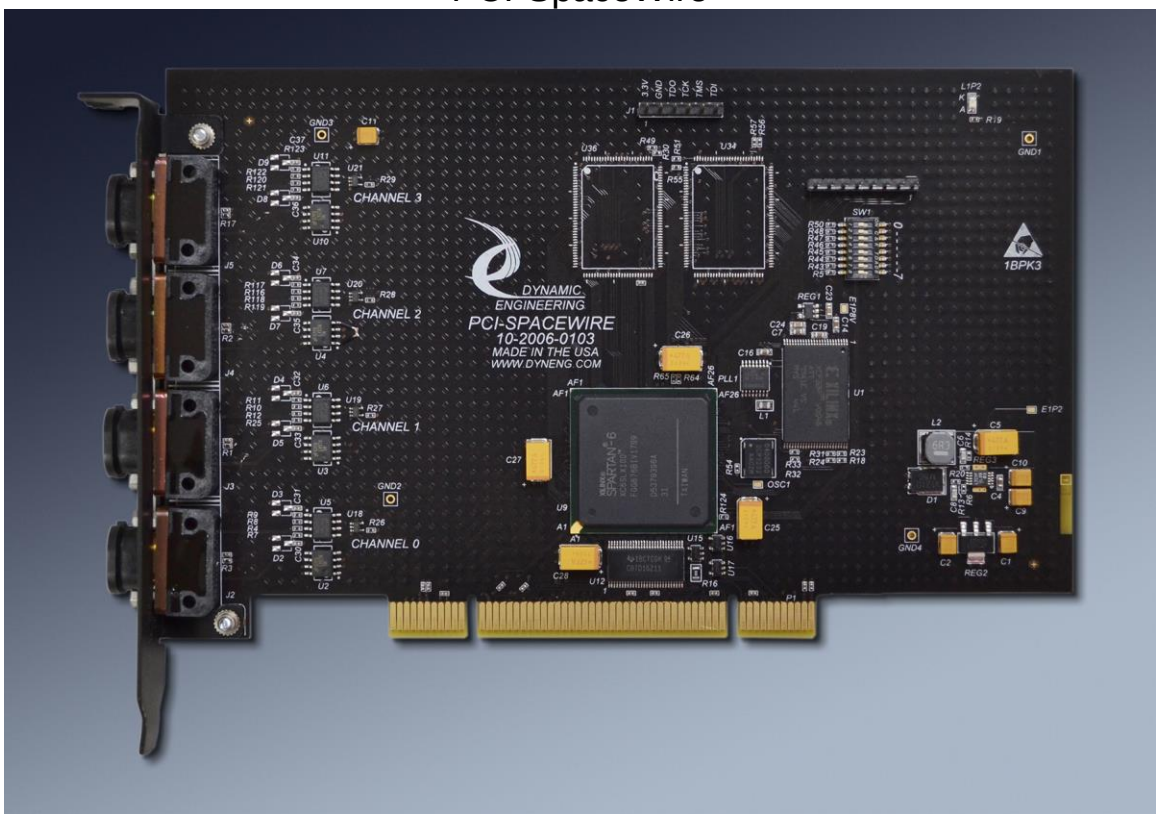
User Manual

SpaceWire "BK" Model Hardware Manual

Four-Channel SpaceWire Interface PCIe, PCI, PC104p, PMC Versions

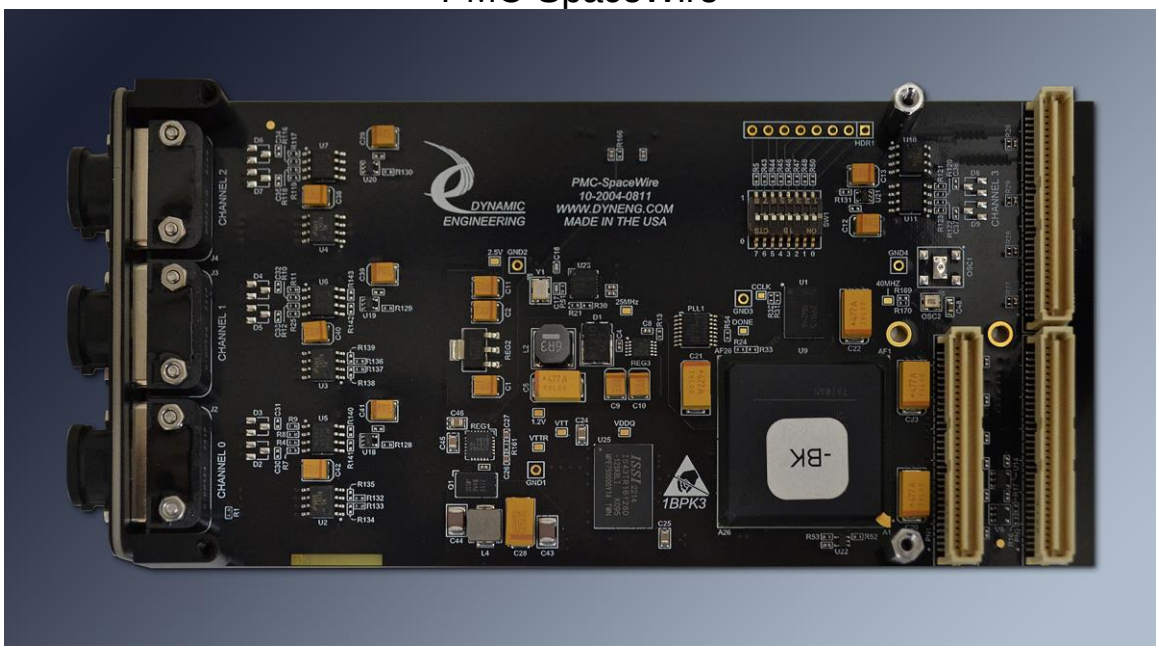
Manual Revision 4p0

PCI-SpaceWire



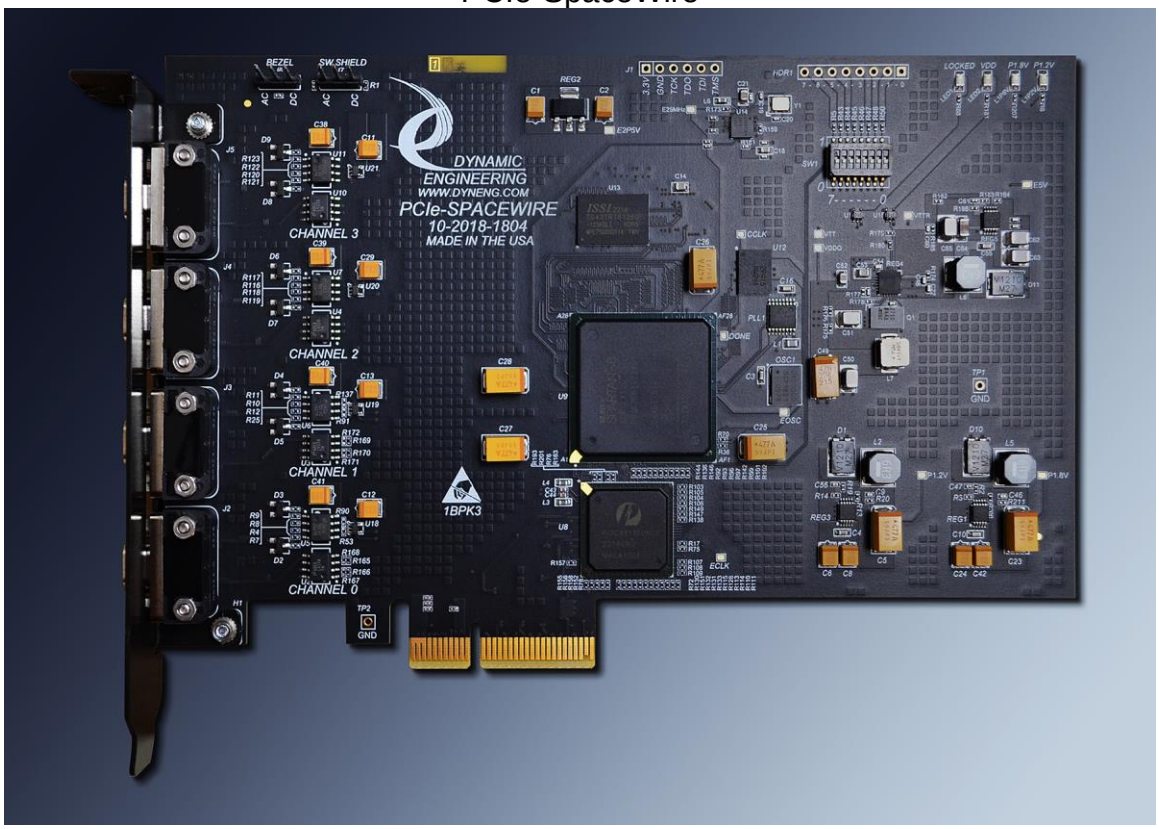
Corresponding Hardware: 10-2006-01(04)

PMC-SpaceWire



Corresponding Hardware: 10-2004-0811

PCIe-SpaceWire



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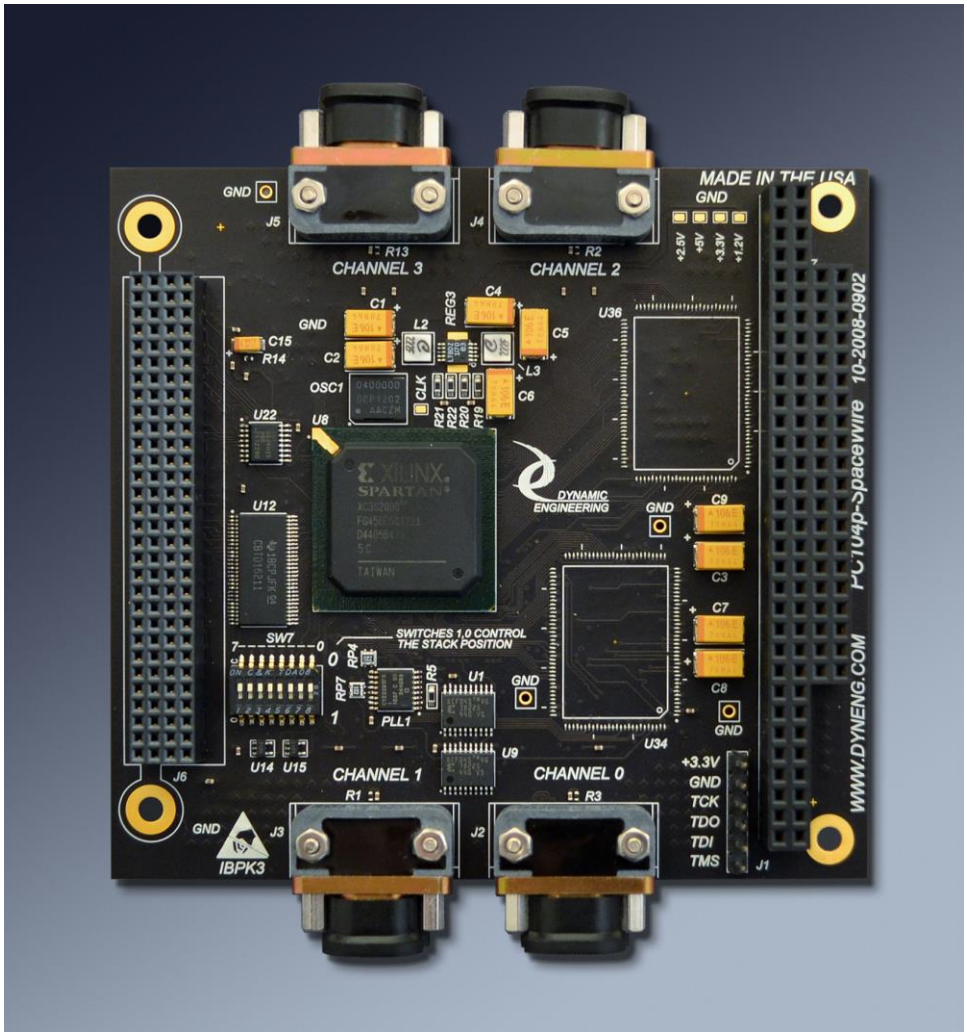

Corresponding Hardware: 10-2008-09(04)

SpaceWireBK
PMC, PCIe, PCI, PC104p versions

Four-Channel SpaceWire Interface

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Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

Table of Contents

List of Figures

Product Description

SpaceWire is part of the Dynamic Engineering family of modular I/O. This manual describes the “BK” family of SpaceWire. Currently PCIe, PCI, PC104p, and PMC versions are available. Please refer to the K family manual for information about the original memory map models.

Each has identical functionality with some variation in the IO connectors. Four ports are supported per card, each with internal FIFO and separate DMA engines to support high speed operation.

To receive the newer version covered in this manual add “-BK” to the part number.

K refers to the last planned update to the original SpaceWire design. Beyond K “BK” is the new version. Since the original PN is called out in client documentation and since the BK version has an updated memory map Dynamic Engineering decided to require the –BK addition to the PN to avoid mistakes in ordering.

External FIFOs can be installed for additional storage capability. Options are available to have the external FIFO attached to channel 0 RX and TX or channels 0 and 1 RX only.

DDR is being added to the designs.

Revision 04 and later PCI-SpaceWire fab required for BK

Revision 04 and later PCIe-SpaceWire PCB required for BK with DDR.
Revision 11 and later PMC-SpaceWire PCB required for BK with DDR.
Revision 04 and later PCI-104-SpaceWire PCB required for BK with DDR.

Additional features of BK models:
1. Larger - 16Kx32 FIFOs for Rx and Tx data storage per channel
2. Updated PLL programming interface
3. Updated memory map to allow for additional features
4. Expanded Time Code time base - 32 bits instead of 20
5. Larger possible segment size for DMA.
6. 200 MHz operation 70C [PLL output is limited to 166 MHz for 85C]
7. Industrial Temperature components
8. Big Endian lane swapping for DMA transfers – selectable option in SW.
9. DDR models have 128Mx16 allocated 8Mx32 per port.

The following diagram shows the “BK” SpaceWire configuration (non-DDR versions):

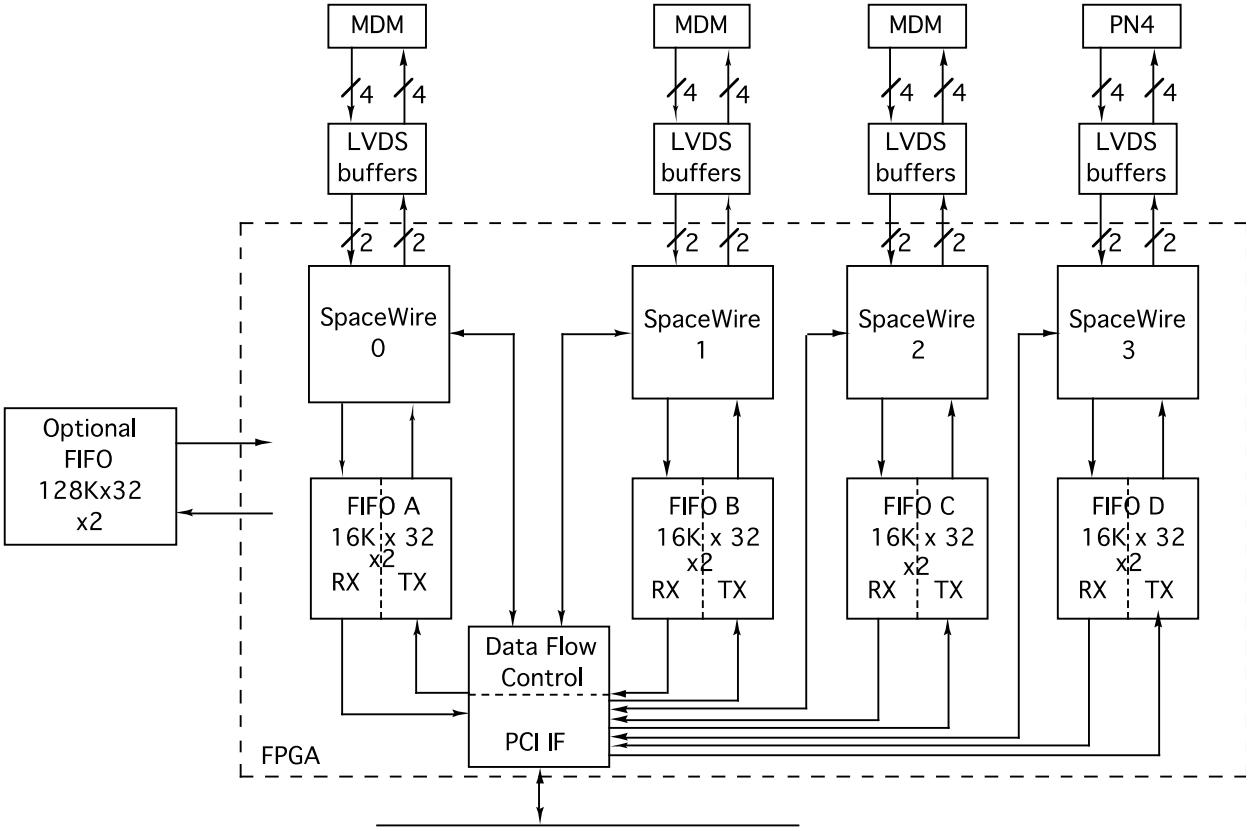


FIGURE 1 SPACEWIRE BK BLOCK DIAGRAM

Note: Figure 1 and 2 do not show the Packet FIFOs which are 1K x 32 per channel per direction [8] to store packet sizes for transmission or definitions from reception and the PLL support FIFOs and/programming engine.

The following diagram shows the “BK” SpaceWire configuration (DDR versions):

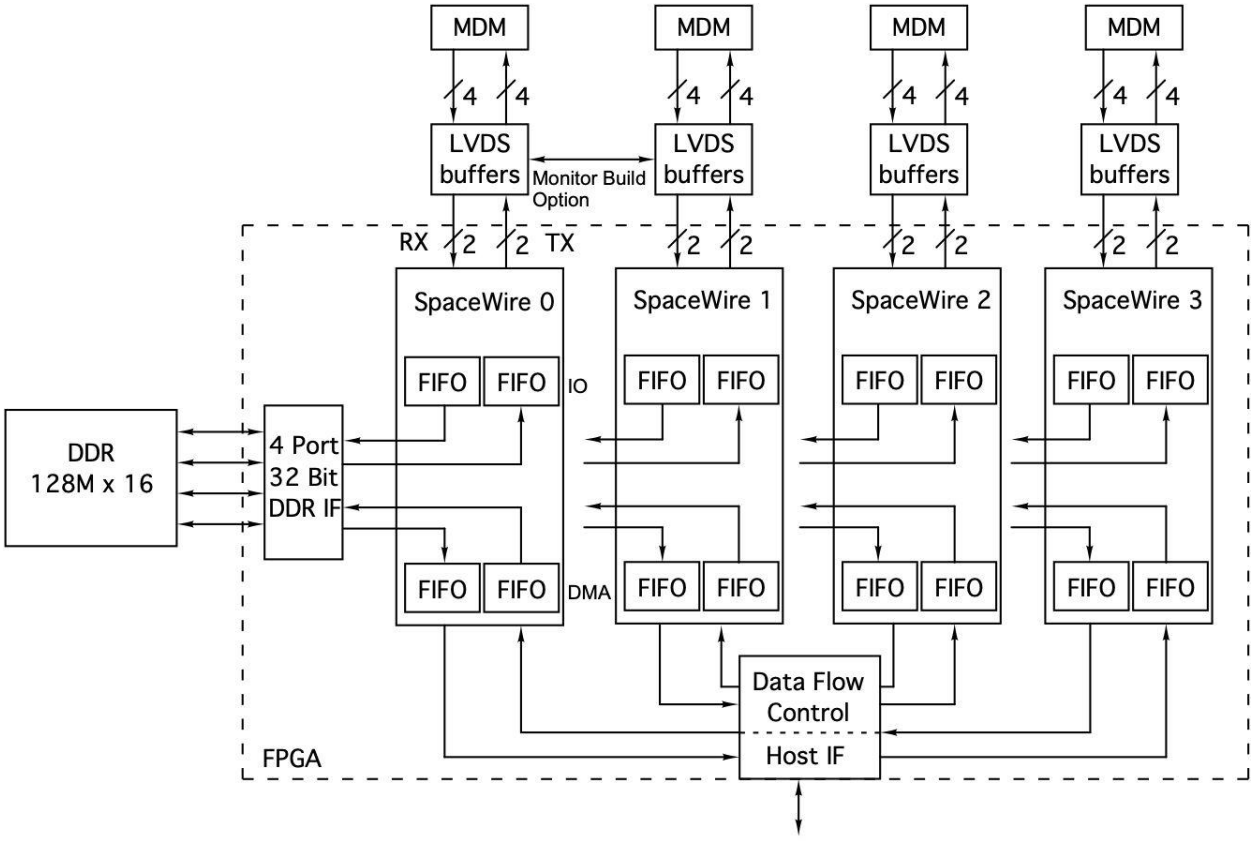


FIGURE 2 SPACEWIRE BK DDR BLOCK DIAGRAM

The port 3 connector implementation varies depending on the format. The PMC version can be configured with 3 MDM connectors, and have 1 channel on Pn4 or all 4 channels routed to Pn4. In all cases, high speed, differential routing with controlled impedance and matched lengths are used for the SpaceWire signaling. It is recommended to use a SpaceWire compatible cable to interconnect your hardware. Dynamic Engineering has several standard lengths of cable and offers custom lengths as well. https://www.dyneng.com/SpaceWireCable.html

If you can use the SpaceWire hardware set but need an alternate protocol please contact Dynamic Engineering. We will redesign the state machines and create a custom interface protocol. See our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

The SpaceWire protocol implemented provides Low Voltage Differential Signaling (LVDS) data inputs and outputs. The transmit data rate is selected by a combination of the programmed output frequencies of the PLL and the divisor values in the channel control registers. The PLL is programmed via software over a serial I2C interface. Transmit data rates are selectable from 2 Mbps to 200 Mbps. The receiver will automatically adjust to the data rate seen.

The SpaceWire specification requires that the transmit frequency be 10 Mbps during the link connection process. In order to accommodate this, the PLL frequency should be at least close to a multiple of 10 MHz. Once the link protocol has established a connection, the transmit speed will convert to the desired transmit rate specified in the channel control registers.

Four independent SpaceWire ports are provided per card. Each SpaceWire port has two LVDS signal pairs for input and two LVDS signal pairs for output. The electrical interface for SpaceWire is as specified in document ECSS-E-50-12C, published by the European Cooperation for Space Standardization dated 31 July 2008. Connections for the first three/four SpaceWire ports on the card are with MDM style connectors as required by the specification.

For PMC and XMC devices the bezel restricts the number of ports at the bezel. The 4th port is presented on the rear IO. Any or all of the four ports can be routed to the rear IO connector rather than the MDM connectors. Isolation and stub control is provided by 0Ω jumpers.

PMC-SpaceWire uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the PMC-SpaceWire, please let us know. We may be able to do a special build with a different height connector to compensate.

All formats available and planned will have a common software interface allowing for porting between systems. Dynamic Engineering offers drivers and reference software for Windows®, Linux, and VxWorks.

Each SpaceWire channel is supported by two 16K by 32-bit FIFOs. The TX FIFOs support long-word writes and the RX FIFOs support long-word reads. For testing, a FIFO test bit in each channel control register enables the data to be routed from the TX to the RX FIFO for a full 32-bit path. DMA operation is supported in both test and operational modes.

DDR models have different configuration with 4 smaller 1Kx32 FIFOs to handle the immediate IO and DMA requirements with the DDR path between them. When the loop-back mode is enabled, the TX IO FIFO is looped back to the RX IO FIFO.
Tx DMA FIFO => DDR => TX IO FIFO => RX IO FIFO => DDR => RX DMA FIFO is the resulting path.

The DDR segments are allocated within the same device using different memory ranges. The ranges default to provide the same amount of memory to each port. The allocations are programmable. By having the default values, the HW will operate properly without the need to change user SW. See the memory/bit map section for more information.

The DDR operates at a much higher frequency and can easily keep up with the port traffic. There is the possibility of some latency, the rate matching buffers cure this plus provide the rate matching.

Each SpaceWire port can receive SpaceWire packets and store them in the associated IO FIFOs. Each SpaceWire packet will be zero extended to align with 32-bit long words. The actual number of bytes in the packet will be stored in the RX packet-length FIFO [1Kx32] and the Data is stored in the IO FIFO.

The host can poll the FIFO flags or wait for the packet received or RX almost full interrupts. The packet data can be read by the host directly from the RX data FIFO [target or DMA]. All models have hardware implemented flow control using the SpaceWire FCT count to prevent overflow into either the Data or Packet FIFOs automatically.

Each SpaceWire transmit port has a separate TX IO FIFO. The FIFO is written as long words. The number of bytes to be transmitted is specified by writing a byte count to the TX packet-length FIFO [1Kx32]. Provided the connection is established, and the flow control from the destination side has authorized data transfer; whenever TX data and packet-length values are written, the transmitter will send data. A packet disable bit in the channel control register allows the interface to function without packetizing the data. When in this mode the transmitter will send data as soon as it is written to the TX FIFO. This essentially treats the data as one infinite length packet.

More on byte alignment: Transmit bytes are read from byte positions 0->3 byte lane wise [7-0] first, [15-8] second, [23-16] third and [31-24] last and the bytes are transmitted in this order. For message byte-counts not divisible by four, the last long-word is read as described. Any unused bytes are considered padding with the next message starting with the next FIFO long-word. For example, with 7 bytes to send, a word of 4 bytes will be read, then the lower 3 bytes will be read and sent and the 8th byte will be dropped.

In the receive direction the action is similar. Bytes are written as long-words to the RX FIFO. The first byte received is loaded into long-word byte 0 [7-0], then byte 1 [15-8], byte 2 [23-16] and byte 3 [31-24]. Whenever a message does not have a complete long-word to load and the end-of-packet character is received, zero-padding of the unused upper-bytes will occur before the long-word is written to the FIFO.

The SpaceWire design supports interrupts. An interrupt can be configured to occur when the TX FIFO is almost empty, the RX FIFO is almost full, when a SpaceWire packet has been transmitted or received, when a time-code character is received or when an error has occurred. All interrupts are individually maskable, and a channel master interrupt enable is provided to disable all interrupts on a channel simultaneously. The current real-time status is also available from the FIFOs making it possible to operate in a polled mode.

For Command & Control situations direct read-write access to the FIFOs makes sense. The messages tend to be short and the added overhead of setting up DMA is not justified. For data transfer DMA is recommended. Each channel has a separate transmit and receive DMA engine for a total of 8 programmable units. The DMA engines can be programmed for long transfers and handle scatter-gather requirements automatically. With only 1 interrupt to deal with at the end of the transfer it is the lowest overhead transfer method for medium and large transfers. Internal to the design is an 8-channel DMA arbiter which controls which port can access the bus for DMA operation. The arbiter operation is completely automatic.

Theory of Operation

SpaceWire designs are for transferring data from one point to another using the SpaceWire protocol as specified in document ECSS-E-50-12C, published by the European Cooperation for Space Standardization dated 31 July 2008.

Continuous development in the SpaceWire community means fairly frequent updates for new features. Generally new features can be added to a released card with a FLASH update. New features are designed to allow for non-updated software to still function – please set undefined bits to zero when programming to facilitate the migration path.

The BK series SpaceWire board(s) feature a Xilinx FPGA. The FPGA contains the PCI interface, all of the registers, FIFO's and protocol controlling elements of the SpaceWire design. Only the transceivers and clock circuitry are external to the Xilinx device.

A logic block within the FPGA controls the PCI interface to the host CPU. The SpaceWire design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI-core decode before the "terminate with data" state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather DMA is provided in this design. Once the physical address of the first chaining descriptor is written to the DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is set to one if the IO transfer is from the SpaceWire board to host memory, and zero if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

NOTE: The direction bit (bit 1) must be set when the physical address of the first chaining descriptor is written to the DMA pointer register (read DMAs only) or a DMA error will result.

The eight DMA controllers obtain access to the PCI bus by asserting a request to the DMA arbiter. Once a controller is granted PCI access, it keeps the bus until it drops its request. At this point if another controller is requesting the bus, it will be granted access. If multiple DMA controllers are asserting requests, the arbiter grants access in a round-robin pattern.

A controller will drop request when it reaches the end of a scatter-gather list entry or the end of a DMA descriptor acquisition. It will also drop request when a transfer from the device to memory is almost out of data, or when a transfer from memory to the device is almost out of room to store the data, or if it has held the PCI bus for 1024 PCI clocks.

A retry counter is included in the DMA controllers. This counter is incremented whenever the DMA controller initiates a PCI bus-cycle and is cleared whenever the controller drops bus request or a data-word is successfully transferred. If the count reaches 1024, the controller is forced to drop bus request, which allows another controller to gain access. The purpose of the retry counter is to prevent a DMA controller from hanging-onto the PCI bus at the detriment of the other ports.

Several state-machines within the FPGA control the link, FIFOs, data transceivers, and flow-control for each channel. The transmitter and receiver for each channel are interdependent. The transmitter requires flow-control information from the receiver to function and the receiver requires the transmitter to send flow-control tokens to regulate the flow of received data.

In a typical transmit sequence the local receiver receives flow control tokens (FCTs) from the remote node. Each FCT authorizes the local transmitter to send eight N(ormal)-Chars (a data-byte, End-Of-Packet token (EOP) or Error End-of-Packet (EEP)) back to the remote node. An up-down counter is used to keep track of the number of N-Chars authorized, and the number of N-Chars that have been sent. Likewise, the local transmitter sends FCTs to the remote receiver node to enable that node's transmitter to send N-Chars to the local receiver. The number of outstanding FCTs is based on the amount of room available in the receive FIFO with an upper limit of 7 FCTs (56 bytes).

The transmitters will multiplex Time-Code characters, FCT characters, N-characters and NULL characters (in that order of priority) onto the data stream to regulate the flow of data in both directions. At the end of a transmitted packet, the transmitter will append an EOP (or possibly an EEP if relaying a packet with an error) character to the message stream to alert the receiver to the completion of the current packet.

The SpaceWire design uses Data-Strobe encoding where clock and data information are sent on two paired serial links. Exactly one transition occurs in either the data line or the strobe line at the end of each bit period allowing the clock to be recovered from the data strobe pair. The timing is shown in figure 2.

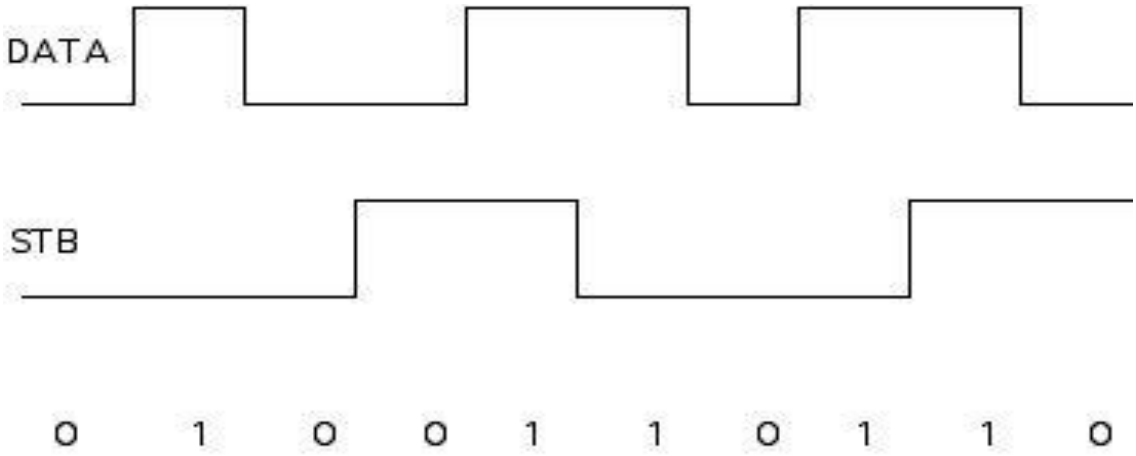


FIGURE 3 SPACEWIRE DATA STROBE ENCODING

Note: SpaceFiber uses a similar mechanism but with 8B10B encoding.

Before the transmitter can start operation, it must establish a link with the connected node. When the link enable control bit is set, the connection state-machine resets the NULL-detected latch and waits 6.4 microseconds before enabling the receiver. The receiver then monitors SpaceWire link activity for 12.8 microseconds. If any link errors or tokens other than NULLs are seen during this period, the receiver is disabled and the process starts over.

At this point the state-machine is in the ready state waiting for a start or auto-start control bit to be set to move to the starting state. The start control bit causes the transmitter to immediately begin sending NULLs and the receiver to look for a NULL in response, whereas the auto-start control bit causes the state-machine to wait for a NULL to be received before transitioning to the starting state and sending NULLs. If a NULL is not seen within 12.8 microseconds while in the starting state, or if errors or tokens other than NULLs are seen, the transmitter and receiver are disabled and the process starts over.

When the transmitter has sent a NULL and the receiver has received a NULL character, the transmitter sends an FCT character and the receiver looks for an FCT in return. If this occurs, it means that the remote node has recognized the NULL and is ready to connect. Once an FCT has been sent and received the link proceeds to the run state.

The transmit frequency is then switched to the requested operational frequency from the 10 MHz connection frequency and Time-codes, FCTs and N-chars (data or end-of-packet tokens) can be sent to and from the node. (See figure 8-2: State diagram for SpaceWire link interface on page 64 of the SpaceWire spec. ECSS-E-ST-50-12C)

The SpaceWire specification allows for a maximum of 56 bytes of credit (seven FCTs) to be outstanding at any time. For each eight bytes that are received, the receiver will request the transmitter to send another FCT as long as sufficient buffer space exists to accommodate the additional data. If the receiver receives a data byte when the outstanding credit is zero, or if an FCT is received that causes the transmit credit to exceed 56 bytes, a credit error has occurred.

The credit error is one of several error conditions that can disrupt the link connection. The others include parity error, disconnect error and escape error. If any of these occur a receive error and the offending error condition status will be latched, the link will disconnect and after a delay, attempt to re-establish the connection.

The parity error occurs when the relevant bits of two successive characters do not constitute odd parity (an odd number of ones). Parity coverage for SpaceWire is offset from the character boundaries by two bits. Although each character begins with a parity bit followed by a data control flag, these two bits are combined with the payload bits from the previous character to determine the parity. The disconnect error occurs when there is no activity on the strobe or data lines to the receiver for a period of 850 nanoseconds. The escape error occurs when an escape character is followed by anything other than an FCT or a data character.

Beginning with Flash Rev 02 STD minor rev 8, 128 & 128RX minor rev5, a Receive Packet FIFO control register was added to select when to back pressure the link to prevent receive packet FIFO overflows from occurring. This improvement effectively removes a SW race condition for small packets[1]. The register can be set to 0x3FF or

[1] If the controlling processor does not keep up with the Packet received interrupts the Packet FIFO would overflow and descriptors lost. The HW update adds the Packet FIFO status to the FCT calculations to prevent overflow.

0x000 to operate in legacy mode. A receive FIFO overflow will also cause a receive error to be latched, but will not in itself cause a link disconnect.

If a receive data-packet is in progress when an error occurs, the receiver ceases writing data to the receive data FIFO and writes the receive packet-length FIFO with the current byte-count with the packet error bit set. If this packet fragment is to be relayed to a remote node, it should be terminated with an EEP rather than an EOP.

If a transmit packet was in progress when the error occurred, the transmitter stops sending data and attempts to purge the remainder of the current packet from the transmit FIFO. Data must be read from the FIFO at the rate of 132 bytes per microsecond, rather than using the FIFO reset, to avoid deleting data belonging to subsequent packets.

A 30 microsecond delay is provided for this purpose, however, if the packet-length is large or if all the packet data is not currently present in the transmit FIFO, the transmitter will be unable to complete the data purge within the 30 microsecond period and the link state-machine will go ahead and disable the receiver and transmitter in preparation for reestablishing the link. The remote receiver that is receiving the data will detect an error when the link is disabled, if it has not already, and will be aware that the packet has been prematurely terminated.

This will clear the transmitter and receiver error state, but a transmitter purge error status bit will be latched to alert the user of this error condition. The user can then read the transmit packet-length FIFO count to determine how many packets are pending, reset the transmit FIFO (which also clears the transmit packet-length FIFO) and perform whatever error recovery is indicated.

See the SpaceWire specification for clarification or elaboration on any of these features.

Programming

Programming the SpaceWire design requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the board is installed. The VendorId = 0xDCBA. The CardId = 0x0055.

Depending on the software environment it may be necessary to set-up the system software with the SpaceWire "registration" data.

If DMA is used it may be necessary to acquire a block of non-paged memory that is accessible from the PCI bus in which to store chaining descriptor list entries. If the Dynamic Engineering device drivers are used, the I/O channel driver will handle all the DMA internal mechanics automatically.

In order to transfer data to another SpaceWire node, several steps must be performed. First a physical connection must be established with the appropriate interface cable. Then the PLL must be programmed to the desired clock configuration. The PLL is connected to the FPGA by an I^2C serial bus. The PLL internal registers are loaded with 40 bytes of data that are derived from a .jed file that can be generated by the CyberClock utility from Cypress semiconductor.

Reference: https://www.dyneng.com/_Download/Utilities/CyberClocks.zip . Select CyClocksRT; the specific PLL part number is CY22393; and the external reference clock frequency is 40 MHz. You can specify frequencies for CLKA – CLKD which supply the I/O reference clocks for channels 0 – 3 respectively. Click the Calculate button and save the file. Newer versions of this utility may be available from Infineon/Cypress.

The SpaceWire card is populated with industrial temperature components. If operating in the Industrial temperature range be sure to set the proper temperature in the CyberClocks software. The upper frequency of the PLL is somewhat limited in Industrial temperature mode. If using for commercial temperature applications, select the commercial temperature range setting to allow for higher operating frequencies.

A four-bit count field in each channel's control register allows the I/O reference clock to be divided by any integer value from 1 to 16 (count values 0 – 0xF) to yield the final operational bit-rate. There is a 5-bit initial count field for each channel in the base control register that is used to divide the I/O reference clock in order to generate the ~10 Mbit per second connection rate. To allow the channels to achieve this connection rate, the PLL should not be programmed to frequencies below 10 MHz and should be at least close to a multiple of 10 MHz.

Routines to program the PLL are included in the driver and UserApp code provided in the engineering kit for the board. The driver will analyze the 40-byte PLL register field to determine the requested frequencies and set the initial count values automatically whenever the PLL is reprogrammed. If you are writing your own driver, contact Dynamic Engineering and we can send you a file with code excerpts from our driver and test software that cover each step of the process.

The link Enable bit and either the Start or Auto-start bit must be set in the channel control register along with the desired operational clock divisor and any interrupt enables that are to be monitored. When the link has been established as reported in the channel status register, data may be written to the transmit FIFO using either single-word writes or DMA. If the packet disable bit has been set, data will be sent as soon as it is written, provided that the receiving node has authorized the transfer. In this mode the data is treated as a single infinite-length packet.

If packetizing is not disabled, the data will not be sent until a packet-length has been written to the SPWR_CHAN_TX_PKT_LEN FIFO. If the packet-length is not divisible by four, the remainder of the last 32-bit FIFO word will be ignored and the next packet's data will begin with the next FIFO word. A packet-length must be written for each packet to be sent, unless the constant packet-length control bit is set. If this bit is set, the first packet-length read will be used continuously until either the data in the transmit data FIFO is exhausted or the constant packet-length control bit is cleared.

Once the link has been established, the receiver will automatically adapt to the frequency of the remote node's transmitter. As data is received, a 32-bit data word will be written to the receive FIFO for every four bytes that are received. When an end-of-packet character is received, the remainder of the received data will be written to the FIFO regardless of whether four bytes have been received (the unused bytes are written as zeros) and the received packet-length (byte count) will be written to the SPWR_CHAN_RX_PKT_LEN FIFO. The packet done bit will also be set and an interrupt generated, if it has been enabled.

Firmware Updates

Revision A: First release of BK. See feature table for new features. 8/14
Revision B1: Second release of BK. Updated for new FPGA pinout, external clock recovery, PMC rear IO connector redefined to match ccPMC version. Add lane steering for DMA in Big Endian systems. 3/16/15
Revision B2: minor update for better internal timing 12/15
Revision B2 : -128 original release based on B2 version standard product.
Revision B3-5: 9/2016 Fine tuning of FPGA terminations and timing based on new layout with built in clock offset for improved hold time. Added minor revision field to status.
⇔ Switch to numerical revisions
Revision 02p8 STD, 02p5 128 & 128RX: Implemented Receive Packet FIFO control register and logic to each channel. Changed PCI bus access logic, FIFO Full logic, and added timer to prevent bus lockups. Drivers changed TSI 384 bridge settings to prevent cache coherency issue in certain system configurations. Added Channel Credit & Time Code Status register to each channel.

Revision 10p1 CreateType 4 with DDR added, FIFO option removed. 2/29/24 [completed FAI]

Address Map

Register Name	Offset Description
SPWR_BASE_CNTRL	0x0000 // 0 Base control register
SPWR_USER_SWITCH	0x0004 // 1 User switch & status read port
SPWR_TIME_CNTRL	0x0008 // 2 Time control register
SPWR_TIME_COUNT	0x000C// 3 Time Code update rate
SPWR_PLL_FIFO	0x0010 // 4 Write to PLL programming FIFO, Read PLL read-back FIFO
SPWR_PLL_STATUS	0x0014 // 5 Status associated with PLL programming
SPWR_CHAN_CNTRL	0x0000 // 0 Control register
SPWR_CHAN_STATUS	0x0004 // 1 Status register
SPWR_CHAN_FIFO	0x0008 // 2 TX/RX FIFOs single word access
SPWR_CHAN_WR_DMA_PNTR	0x000C // 3 write DMA physical PCI dpr address
SPWR_CHAN_TX_FIFO_COUNT	0x000C // 3 transmit FIFO data count
SPWR_CHAN_RD_DMA_PNTR	0x0010 // 4 read DMA physical PCI dpr address
SPWR_CHAN_RX_FIFO_COUNT	0x0010 // 4 receive FIFO data count
SPWR_CHAN_TX/RX_PKT_LEN	0x0014 // 5 Write TX/Read RX packet-length
SPWR_CHAN_TX_AMT	0x0018 // 6 TX almost empty level
SPWR_CHAN_RX_AFL	0x001C // 7 RX almost full level
SPWR_CHAN_CREDIT_TC_STATUS	0x0020 // 8 Credit and TimeCode Status register
SPWR_CHAN_RX_PKT_FF_FULL_CNTL	0x0024 // 9 RX Packet FIFO Full Control register
Type 4 models only	
SPWR_CHAN_TX_DDR_FIFO_CNT	0x0028 // 10 Tx FIFO count including DDR
SPWR_CHAN_RX_DDR_FIFO_CNT	0x002C // 11 Rx FIFO count including DDR
SPWR_CHAN_BURST_IN_PTR	0x0030 // 12 Tx DMA Current Pointer
SPWR_CHAN_BURST_OUT_PTR	0x0034 // 13 Rx DMA Current Pointer
SPWR_CHAN_TX_STRT_ADD	0x0038 // 14 Tx Start Address – DDR allocation
SPWR_CHAN_TX_STOP_ADD	0x003C // 15 Tx Stop Address – DDR allocation
SPWR_CHAN_RX_STRT_ADD	0x0040 // 14 Rx Start Address – DDR allocation
SPWR_CHAN_RX_STOP_ADD	0x0044 // 15 Rx Stop Address – DDR allocation

FIGURE 4 SPACEWIRE ADDRESS MAP

Channel definitions repeat. Each port having the internal offsets shown plus the following table. All are relative the assigned BAR0 address.

Port 0 0x050
Port 1 0x0A0
Port 2 0x0F0
Port 3 0x140

Register Definitions

SPWR_BASE_CNTL

[0x0000] Base Control Register (read/write)

Base Control Register

Data Bit	Description
31	BigEndianDma
30	IoRst
29-28	Time-Code Control Flags
27-25	Spare
24	PLL USE ALT
23	PLL CHK
22	PLL RD
21	PLL RST
20	PLL Enable
19-15	IO Clock D Initial Divisor
14-10	IO Clock C Initial Divisor
9-5	IO Clock B Initial Divisor
4-0	IO Clock A Initial Divisor

FIGURE 5 SPACEWIRE BASE CONTROL REGISTER

All bits are active high and are reset on system power-up or reset, except PLL enable, which defaults to enabled (high) on power-up or reset.

IO Clock A-D Initial Divisor: These four fields determine the divisor used to generate the 10 MHz connection clock rate. IO clock A is used for channel 0, IO clock B is used for channel 1, IO clock C is used for channel 2 and IO clock D is used for channel 3. Depending on the frequencies programmed into the PLL, different divisors are required to achieve the 10 MHz bit-rate required by the SpaceWire specification for establishing the link connection. These fields specify those divisors. The frequency divisor is actually one more than the value entered. A value of zero corresponds to a divisor of one. A value of one corresponds to a divisor of two etc. If the Dynamic Engineering device driver is used, these values are written automatically when the PLL is programmed.

PLL Enable: When this bit is set to a one, the signals used to program and read the PLL are enabled.

PLL RST: When Set ‘1’ causes a reset to the PLL programming HW.

PLL RD: when set selects reading the PLL, when cleared selects writing to the PLL registers.

PLL_CHK: Set to check PLL address.

PLL USE ALT: When set selects the Alternate PLL address. 0 => x69, 1 => x6A

Time-Code Control Flags: These two bits are added to the six-bit time count in bit positions 7 and 6. Their purpose is currently not defined in the SpaceWire specification.

IoRst when '1' causes a reset to the DDR controller for each of the 4 ports. Separate port only resets are available within the port. '0' for normal operation.

BigEndianDma : '0' disables this option. '1' enables this option. When operating with a Big Endian platform and using PCI accesses DMA can have challenges. The register accesses directly over the PCI bus are usually taken care of automatically with byte swapping within the CPU or PCI interface on the CPU. DMA data is written to or read from the local memory and is not swapped. The direct read/write from memory ends up with scrambled data [relative to SpaceWire little endian definitions]. Setting this bit will byte reverse the data for the DMA path into the Tx and out of the Rx FIFO's only. Register accesses are not affected.

31-24, 23-16, 15-8, 7-0 ⇔ 7-0, 15-8, 23-16, 31-24 byte swapping pattern implemented.

SPWR_USER_SWITCH

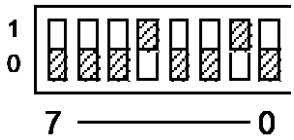
[0x0004] User Switch Port - read only

Dipswitch Port

Data Bit	Description
31	Calibration Done
30-28	Spare
27	Channel 3 Interrupt Active
26	Channel 2 Interrupt Active
25	Channel 1 Interrupt Active
24	Channel 0 Interrupt Active
23-20	Xilinx Design Revision Minor
19-16	Xilinx Design Configuration Type
15-8	Xilinx Design Revision Number Major
7-0	Switch Setting

FIGURE 6 SPACEWIRE USER SWITCH PORT

Switch 7-0: The user switch is read through this port. The bits are read as the lowest byte. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example, the switch figure below indicates a 0x12.



Channel 0-3 Interrupt Active: When a one is read, it indicates that the corresponding channel's interrupt is active. When a zero is read, that interrupt is inactive.

Calibration Done: on models with DDR this bit indicates the DDR initialization process has completed successfully. Also note the blinking LED indicating the DDR clock controller is locked onto the reference and supplying the required high speed clock outputs.

Xilinx Design Configuration Type Major and Minor and Xilinx Design Revision Number: These values of the describe the channel configuration and revision of the Xilinx design.

Currently there are 4 configurations for the HW with the following definitions
note: as the DDR update is added to the form factors supported and current stock is depleted the DDR model will be shipped to all orders. In the meantime if your design requires the DDR type please ask for it.

0 => Spare

1 => S6 with internal 64 Kbyte data FIFOs and Two G byte maximum packet-lengths for all channels.

2 => S6 with internal 64 Kbyte data FIFOs and Two G byte maximum packet-lengths for all channels.
Plus external 128Kx32 FIFO's on for Channel 0 RX & Tx

3 => S6 with internal 64 Kbyte data FIFOs and Two G byte maximum packet-lengths for all channels.
Plus external 128Kx32 FIFO's on for Channel 0 & 1 RX.

4 => S6 with DDR plus 2, 1K FIFOs per path. Default of 32Mbytes per Rx or Tx port [DDR]. Miscellaneous enhancements to minimize latency and increase utility.

5-F => Spare

The Major Revision field is the released name for the particular revision. The Minor Revision field is for Dynamic Engineering revision tracking during development, and for minor released updates between Major Updates.

SPWR_TIME_CNTRL

[0x0008] Time Control Register (read/write)

Time Control Register

Data Bit	Description
31-15	Spare
14-12	Channel 3 Time-Code Source Control
11	Spare
10-8	Channel 2 Time-Code Source Control
7	Spare
6-4	Channel 1 Time-Code Source Control
3	Spare
2-0	Channel 0 Time-Code Source Control

FIGURE 7 SPACEWIRE TIME CONTROL REGISTER

All bits are active high and are reset to zero on system power-up or reset.

Channel 0-3 Time-Code Source Control: These four fields control the source of the time-code signals for the four channels as follows:

"000"-> Disabled: Time-code characters are not sent by this channel.

"001"-> Master: Time-code characters for this channel come from the master timer and time-code counter.

"010"-> Channel 0: Time-code characters received by channel 0 are subsequently sent by this channel.

"011"-> Channel 1: Time-code characters received by channel 1 are subsequently sent by this channel.

"100"-> Channel 2: Time-code characters received by channel 2 are subsequently sent by this channel.

"101"-> Channel 3: Time-code characters received by channel 3 are subsequently sent by this channel.

Write 0-5 to each of the fields to select the source for that channel. For example, writing the "101" pattern to channel 0 will have the time code received by channel 3 passed to channel 0 for retransmission. To use the local master use code "001" and so forth.

SPWR_TIME_COUNT

[0x000C] Time Count Register (read/write)

Time Control Register	
Data Bit	**Description**
31-0	Master Timer Divider Count

FIGURE 8 SPACEWIRE TIME COUNT REGISTER

Master Timer Divider Count: This count is used to generate the TICK_IN signal when a channel is used as the source for time-codes. The counter is clocked by the 80 MHz link clock and this count represents the count at which the counter resets to zero, increments the time-code and issues a TICK_IN signal. If this field is set to zero, the six-bit time-code counter and the 32-bit tick timer are reset to zero; when the count is set to a non-zero value, counting proceeds. The 32-bit counter allows a maximum time between ticks of approximately 53.68 seconds.

Normally the timer is set to a much lower value, 1 mS for example. Program for N-1 to be exact since the count runs from 0-> programmed value and then back to 0.

SPWR_PLL_FIFO

[0x0010] PLL Data FIFO (read/write)

PLL Data FIFO	
Data Bit	**Description**
31-0	Data to PLL or Data From PLL

FIGURE 9 SPACEWIRE PLL DATA FIFO

SpaceWire has an improved I2C interface for programming the PLL. Dynamic Engineering driver support packages include utilities to take the .jed file from the Cypress CyberClocks program, parse and load into the FIFO with the proper sequence of controls via Base Control Register. Please see the reference code for the sequence. Linux, VxWorks, Win10/11 packages.

The data to program the PLL is written to this address. The hardware has a state-machine to read the data from the FIFO and load into the PLL. Similarly, the state-machine can read the data from the PLL and write it to the read side FIFO.

SPWR_PLL_STATUS

[0x0014] PLL Status (read/write)

Time Control Register	
Data Bit	**Description**
31-10	Spare
10	PLL Error Latched
9	PLL Done Latched
8	PLL Ready
7	Spare
6	PLL FIFO RX Data Valid
5	PLL FIFO RX FULL
4	PLL FIFO RX EMPTY
3	Spare
2	PLL FIFO TX Data Valid
1	PLL FIFO TX FULL
0	PLL FIFO TX MT

FIGURE 10 SPACEWIRE PLL STATUS REGISTER

The PLL Status bits are used to as feed-back to control the transfer of data to and from the PLL FIFO. TX refers to programming the PLL and RX refers to reading back from the PLL.

The Latched Bits {10,9} are held until cleared by writing back with the bit position(s) set. Usually these bits are cleared before starting an operation.

PLL FIFO TX MT is set when the programming FIFO for the PLL is empty.

PLL FIFO TX FULL is set when the programming FIFO for the PLL is full.

PLL FIFO TX Data Valid is set when data is valid in the pipeline between the FIFO and the State –Machine. The bit is cleared each time the data is read. During operation this bit will toggle to provide some indication that the transfer is occurring.

PLL FIFO RX Empty is set when the read-back FIFO for the PLL is empty.

PLL FIFO RX FULL is set when the read-back FIFO for the PLL is full.

PLL FIFO RX Data Valid is set when Data is valid in the output port for the PLL read path. Data is pre-read from the FIFO and held in the FIFO holding register. The FIFO can be Empty and still have 1 word left in the holding register if Valid is still set.

PLL Done Latch is set when the transfer is completed. This bit can be polled to know when the PLL has been programmed or when the PLL has been read. Please note: The PLL settling time is in addition to the transfer time. Several mS should be delayed after programming the PLL to make sure the specified frequencies are within range. 10 mS is recommended.

PLL Error Latched is set when an error is detected in the I2C transfer. The main purpose for this bit is in discovery for the address of the PLL. The Address can be x6A or x69. Once the correct address is known this bit should be checked but not set. Sticky bit, write with bit position set to clear.

SPWR_CHAN_CNTRL_0-3

[0x0050, 0x00A0, 0x00F0, 0x0140] Channel Control Register (read/write)

Channel Control Register

Data Bit	Description
31	Read DMA Ready (read only)
30	Write DMA Ready (read only)
29-28	Time-Code Flags (read only)
27	DDR Disable for type 4.
26	Spare
25	Return Valid Packet-Lengths Only Enable
24	Transmit Packet-Length Repeat
23	Receive FIFO Programmable Level Load
22	Transmit FIFO Programmable Level Load
21	Read DMA Arbitration Priority Enable
20	Write DMA Arbitration Priority Enable
19	Read DMA Interrupt Enable
18	Write DMA Interrupt Enable
17	Force Interrupt
16	Master Interrupt Enable
15	Tick Received Interrupt Enable
14	Packet Received Interrupt Enable
13	RX Error Interrupt Enable
12	RX Almost Full Interrupt Enable
11	TX Almost Empty Interrupt Enable
10	Packet Disable
9	Link Auto-Start
8	Link Start
7	Link Enable
6	FIFO Loop-Back Enable
5	Receive FIFO Reset
4	Transmit FIFO Reset
3-0	IO Clock Divisor

FIGURE 11 SPACEWIRE CHANNEL CONTROL REGISTER

All bits are active high and are reset on system power-up or reset.

IO Clock Divisor: This field determines the divisor used to generate the operational clock rate. The frequency divisor is actually one more than the value entered. A value of zero corresponds to a divisor of one, one corresponds to a divisor of two etc.

Transmit/Receive FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO, packet-length FIFO and control and status circuitry will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are referenced to the PCI clock, two periods are required for proper reset.

FIFO Loop-Back Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without connecting to another SpaceWire node. When this bit is zero, normal operation is enabled.

Link Enable: When this bit is set to a one, the link connection process will be initiated. The connection state-machine will proceed to the Ready state until Start or Auto-Start is asserted. When this bit is zero, the link connection will be disabled.

Link Start: When this bit is set to a one, the link state-machine will move from the Ready state to the Started state and will attempt to establish a connection with another node. When this bit is zero, the state-machine will remain in the Ready state, provided it has already achieved this state. Once the state-machine has left the Ready state, this bit has no effect.

Link Auto-Start: The behavior of this bit is similar to Link start, however, when this bit is set and Link start is not set, the state-machine will not proceed to the Started state unless a Null character has been seen, which indicates that the other node is attempting to establish a connection. This bit allows the connection process to be cleanly initiated from one side of the link only.

Packet Disable: When this bit is set to a one, data is transferred without being separated into packets. No end-of-packet characters are generated or received and the packet-length FIFOs are not used. As soon as data is written to the transmit FIFO it will be sent out, provided all other conditions allow this. When this bit is zero, the data will be sent in packets. Data must be written to the transmit data FIFO and packet lengths must be written to the TX packet-length FIFO, before data can be transferred.

TX Almost Empty Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level becomes equal or less than the value specified in the SPWR_CHAN_TX_AMT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX Almost Full Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level becomes equal or greater to the value specified in the SPWR_CHAN_RX_AFL register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX Error Interrupt Enable: When this bit is set to a one, an interrupt will be generated when a receiver error condition is detected, provided the channel master interrupt enabled is asserted. When a zero is written to this bit, an interrupt will not be generated, but the latched status can still be read from the channel status register.

Packet Received Interrupt Enable: When this bit is set to a one, an interrupt will be generated when a complete packet is received, provided the channel master interrupt enable is asserted. When a zero is written to this bit, an interrupt will not be generated, but the latched status can still be read from the channel status register.

Tick Received Interrupt Enable: When this bit is set to a one, an interrupt will be generated when a valid time-code is received, provided the channel master interrupt enable is asserted. When a zero is written to this bit, an interrupt will not be generated, but the latched status can still be read from the Interrupt Status register.

Master Interrupt Enable: When this bit is set to a one all enabled interrupts for the referenced channel (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one a system interrupt will occur provided the channel master interrupt enable is set. This is useful to test interrupt service routines.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA write and read completion for the referenced channel. These two interrupts cannot be disabled by the master interrupt enable.

Write/Read DMA Arbitration Priority Enable: These two bits, when set to one, enable the DMA arbiter to use the TX almost empty and/or RX almost full status to give priority to a channel that is approaching the limits of its FIFOs. The levels written to the TX almost empty and RX almost full registers are used to determine these status values. When these bits are zero normal round-robin arbitration is used to determine access to the PCI bus for DMA transfers.

Transmit/Receive FIFO Programmable Level Load: These bits are only valid for channels with external data FIFOs. The load bits must be active during FIFO reset to select the programmable level feature. Once selected, these bits must be set to zero for normal FIFO operation. When set to one, data accesses are instead directed to the almost empty and almost full level registers (See FIFO data sheet for details).

Transmit Packet-Length Repeat: When this bit is set to a one, the current transmit packet-length will be used continually until there is no more transmit data or this control bit is cleared. When a zero is written to this bit, the packet-length FIFO must be read to obtain a new packet-length for each transmitted packet.

Return Valid Packet-Lengths Only Enable: When this bit is set to a one, only valid packet-lengths will be returned. If no new packet has been received since the packet-length FIFO was read, the packet-length will be returned as zero. When a zero is written to this bit and no new packet has been received since the packet-length FIFO was read, the packet-length from the last packet received will be returned. When enabled, this control allows packet-lengths to be confidently read without first checking the Receive Packet Length Valid status bit in the channel status register. This control bit was added starting with rev. J.

DDR Disable: For DDR equipped models this bit when set disables the port's DDR controller. The reset / default condition is enabled. To change values for segments the controller should be disabled. The new parameters entered, and then re-enabled to resume operation. It is recommended to reset the DDR after the parameters are changed to make sure the controller starts up within the defined space. See the Start/End registers for more information. *Note: the read-back value is inverted. '1' = enabled and '0' = disabled.*

Time-Code Flags: The time-code flags have been moved to the control register to make room for the latched almost empty/full status bits that were added to the status register. These two read-only bits are currently undefined in the SpaceWire specification and will most likely always be seen as zeros.

Write/Read DMA Ready: These two read-only bits report the DMA state-machine status. If they are read as a one, the corresponding DMA state-machine is idle and available to start a transfer. If the bits are read as a zero, the corresponding DMA state-machine is processing a data transfer.

SPWR_CHAN_STATUS_0-3

[0x0054, 0x00A4, 0x00F4, 0x0144] (Status read/Latch clear write)

Channel Status Register

Data Bit	Description
31	Latched Receive FIFO Almost Full
30	Latched Transmit FIFO Almost Empty
29-24	Time-Code Data
23	Interrupt Active
22	Receive Packet Length Valid
21	Transmit Purge Error
20	SpaceWire Link Established
19	Read DMA Error
18	Write DMA Error
17	Read DMA List Complete
16	Write DMA List Complete
15	TICK_OUT Received
14	Packet Received
13	Receive Error
12	Receive FIFO Overflow
11	Credit Error Detected
10	Escape Error Detected
9	Disconnect Error Detected
8	Parity Error Detected
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Transmit Data Valid
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 12 SPACEWIRE CHANNEL STATUS REGISTER

Transmit FIFO Empty: When a one is read, the transmit data FIFO for the corresponding channel contains no data; when a zero is read, there is at least one data-word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data-words in the transmit data FIFO for the corresponding channel is less than or equal to the value written to the SPWR_CHAN_TX_AMT register for that channel; when a zero is read, the level is more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO for the corresponding channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Transmit Data Valid: When a one is read, there is at least one word of valid transmit data. When either the transmitter or the FIFO bypass is enabled, the first word written to the transmit FIFO will be read to be available to the transmitter or the FIFO bypass circuit. Therefore although the FIFO is empty, if this bit is set, there is one additional long-word of transmit data. A zero indicates that there is no valid transmit data.

Receive FIFO Empty: When a one is read, the receive data FIFO for the corresponding channel contains no data; when a zero is read, there is at least one data-word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data-words in the receive data FIFO for the corresponding channel is greater or equal to the value written to the SPWR_CHAN_RX_AFL register for that channel; when a zero is read, the level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO for the corresponding channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Receive Data Valid: When a one is read, there is at least one word of valid receive data. When data is written to the receive FIFO, the first four words are read and held in latches to be ready for a PCI read DMA or single-word read. Therefore although the FIFO is empty, if this bit is set, there are as many as four additional long-words of receive data. A zero indicates that there is no valid receive data.

Parity Error Detected: When a one is read, it indicates that a parity error has occurred since the status was last cleared. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no parity error has occurred.

Disconnect Error Detected: When a one is read, it indicates that a disconnect error has occurred since the status was last cleared. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no disconnect error has occurred. A disconnect error occurs when there is no activity on the data or strobe line for 850 nanoseconds.

Escape Error Detected: When a one is read, it indicates that an escape error has occurred since the status was last cleared. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no escape error has occurred. An escape error occurs when an escape character is followed by anything other than an FCT or a data character.

Credit Error Detected: When a one is read, it indicates that a credit error occurred since the status was last cleared. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no credit error has occurred. A credit error is a violation of the SpaceWire data flow-control protocol.

Receive FIFO Overflow: When a one is read, it indicates that either an attempt has been made to write data to a full receive data FIFO or a packet-length value to a full packet-length FIFO. Neither of these conditions should occur if the data flow-control protocol is functioning correctly. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no overflow condition has occurred.

Receive Error: When a one is read, it indicates that one of the five preceding error conditions has been detected since this bit was last cleared. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no receive error has occurred.

Packet Received: When a one is read, it indicates that a packet has been received since this bit was last cleared. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that a packet has not been received.

TICK_OUT Received: When a one is read, it indicates that a valid time code has been received by the referenced channel since this bit was last cleared. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that a valid time-code has not been received.

Write/Read DMA List Complete: When a one is read, it indicates that the corresponding DMA has completed. These bits are latched and must be cleared by writing the same

bit back to the channel status port. A zero indicates that the corresponding DMA has not completed.

Write/Read DMA Error: When a one is read, it indicates that an error has occurred while the corresponding DMA was in progress. This could be a target or master abort or an incorrect direction bit in one of the DMA descriptors. These bits are latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no DMA error has occurred.

SpaceWire Link Established: A one indicates that the referenced link is in the run state, which allows all types of link and normal characters to be exchanged. A zero indicates that the link is not in the run state.

Transmit Purge Error: When a one is read, it indicates that a connection error occurred while a transmit packet was in progress and the transmitter was unable to completely delete the remainder of the packet's data from the transmit data FIFO. This can occur if the packet-length was longer than 4 Kbytes or the packet data had not been all written to the transmit data FIFO. The link connection state-machine allows a 30 microsecond delay for purging transmit data after a link error. At 132 Mbytes/second this allows almost 4 Kbytes of data to be discarded. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no transmit purge error has occurred.

RX packet Length Valid: When a one is read, there is at least one valid receive packet-length value available. When this bit is a zero, it indicates that there are no valid receive packet-length values.

Interrupt Active: When a one is read, it indicates that an enabled interrupt condition (other than the DMA interrupts) is active for the referenced channel. A zero indicates that no enabled interrupt condition is active.

Time-Code Data: The last time-code value received can be read from this six-bit data-field. The TICK_OUT received status bit will indicate if the data is a new valid time-code value. A time-code is considered valid if it is one more than the previous stored value. If the time-code is the same as the stored value, it is assumed to be a duplicate resulting from a cycle in the SpaceWire network and is therefore ignored. If the time-code meets neither of these conditions, it is stored, but the TICK_OUT signal is not asserted until the next time-code is received and is one more than that last stored value. At this point the time-code is deemed to be re-synchronized.

Latched Receive FIFO Almost Full: When a one is read, it indicates that the receive FIFO data count has become greater than or equal to the value in the

SPWR_CHAN_RX_AFL register. A zero indicates that the FIFO has not become almost full. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Latched Transmit FIFO Almost Empty: When a one is read, it indicates that the transmit FIFO data count has become less than or equal to the value in the SPWR_CHAN_TX_AMT register. A zero indicates that the FIFO has not become almost empty. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

SPWR_CHAN_FIFO_0-3

[0x0058, 0x00A8, 0x00F8, 0x0148] Write TX/Read RX FIFO Ports

RX and TX FIFO Ports	
Data Bit	**Description**
31-0	FIFO Data-Word

FIGURE 13 SPACEWIRE CHANNEL RX/TX FIFO PORTS

These ports are used for single-word accesses into the channel TX FIFO and out of the channel RX FIFO.

SPWR_CHAN_WR_DMA_PNTR_0-3

[0x005C, 0x00AC, 0x00FC, 0x014C] Write only

Input DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 14 SPACEWIRE CHANNEL WRITE DMA POINTER PORT

This write-only port is used to initiate a scatter-gather write [TX] DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. Essentially this data acts like a chaining descriptor value pointing to the next value in the chain.

The first is the address of the first memory block of the DMA buffer containing the data to read into the device, the second is the length in bytes of that block, and the third is

the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

All three values are on LW boundaries and are LW in size. Addresses for successive parameters are incremented. The addresses are physical addresses the HW will use on the PCI bus to access the Host memory for the next descriptor or to read the data to be transmitted. In most OS you will need to convert from virtual to physical. The length parameter is a number of bytes, and must be on a LW divisible number of bytes.

Status for the DMA activity can be found in the channel control register and channel status register.

Notes:

1. Writing a zero to this port will abort a write DMA in progress.
2. End of chain should not be set for the address written to the DMA Pointer Address Register. End of chain should be set when the descriptor follows the last length parameter.
3. The Direction should be set to '0' for Burst In DMA in all chaining descriptor locations.
4. The segment size is 31-0 however the byte count is shifted down two positions to create a LW count in memory. This means the actual count is 1G-1 [4Gbytes minus 1 LW] or xFFFFFFFC for the max byte count.

SPWR_CHAN_TX_FIFO_COUNT_0-3

[0x005C, 0x00AC, 0x00FC, 0x014C] TX FIFO Data Count (read only)

TX FIFO Data Count

Channels with External TX Data FIFOs

Data Bit	Description
31-20	Number of TX Packet-Length Values Stored
19-0	Number of TX Data-Words Stored

Channels with Internal TX Data FIFOs

31-20	Number of TX Packet-Length Values Stored
19-14	Spare
13-0	Number of TX data-Words Stored
Type 4 designs report	
31-20	Number of TX Packet-Length Values Stored
19-14	Spare
9-0	Number of TX data-Words Stored in IO FIFO

FIGURE 15 SPACEWIRE CHANNEL TX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding transmit FIFO. There is an additional latch that may contain data if enabled, which allows this value to be a maximum of 0x4000 for channels with internal transmit data FIFOs or 0x23FFF for a channel with an external transmit data FIFO. Please note: the counts are LW based. x4 for byte counts.

Type 4 implementations require a wider count. The TX IO FIFO is reported [only] in this register. The TX DDR FIFO CNT register has the full path with both DMA and IO FIFOs plus DDR. The IO count in this register is provided to allow for previous SW implementations to be used without modification. It is highly recommended to update to use the new count. The updated drivers return the correct version based on the design type.

The transmit packet-length count field is in this register. This allows the user to know how many packet-length values can be safely written to the packet-length FIFO without causing an overflow. It also aids in error recovery if there was a connection error during a packet transmission and the transmitter is unable to automatically purge the remaining data from the impacted packet. In this case the user must intervene to reestablish a consistent packet/data state by resetting the transmit FIFO and rewriting packet data

and packet-length values. Knowing how many packets were pending when the error occurred will greatly aid in this procedure.

SPWR_CHAN_RD_DMA_PNTR_0-3

[0x0060, 0x00B0, 0x0100, 0x0150] Write only

Output DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 16 SPACEWIRE CHANNEL READ DMA POINTER PORT

This write-only port is used to initiate a scatter-gather read [RX] DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. Essentially this data acts like a chaining descriptor value pointing to the next value in the chain.

The 1st read retrieve the address of the first memory block (DMA buffer) to write to, the 2nd is the length in bytes of that block, and 3rd is the address of the next chaining descriptor in the linked list (buffer memory blocks). This process is continued until the end-of-chain bit of the next pointer value read indicates it is the last chaining descriptor in the list.

All three values are on LW boundaries and LW in size. Addresses for successive parameters are incremented. The addresses are physical addresses the HW will use on the PCI bus to access the Host memory. In most OS you will need to convert from virtual to physical. The length parameter is a number of bytes, and must be on a LW divisible number of bytes.

Status for the DMA activity can be found in the channel control register and channel status register.

Notes:

1. Writing a zero to this port will abort a write DMA in progress.
2. End of chain should not be set for the address written to the DMA Pointer Address Register. End of chain should be set when the descriptor follows the last length parameter.
3. The Direction should be set to '1' for Burst Out DMA in all chaining descriptor locations.
4. The segment size is 31-0 however the byte count is shifted down two positions to create a LW count in memory. This means the actual count is 1G-1 [4Gbytes minus 1 LW] or xFFFFFFFC for the max byte count. **NOTE: The direction bit (bit 1) must be set when the physical address of the first chaining descriptor is written to this register or a read DMA error will result.**

SPWR_CHAN_RX_FIFO_COUNT_0-3

[0x0060, 0x00B0, 0x0100, 0x0150] RX FIFO Data Count (read only)

RX FIFO Data Count

Channels with External RX Data FIFOs

Data Bit	Description
31-20	Number of RX Packet-Length Values Stored
19-0	Number of RX Data-Words Stored

Channels with Internal RX Data FIFO's

31-20	Number of RX Packet-Length Values Stored
19-15	Spare
14-0	Number of RX data-Words Stored
Type 4 designs report	
31-20	Number of RX Packet-Length Values Stored
19-14	Spare
9-0	RX data-Words Stored in DMA FIFO

FIGURE 17 SPACEWIRE CHANNEL RX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding receive FIFO. There are four additional latches in the read DMA pipeline that may contain data, which allows this value to be a maximum of 0x4003 for channels with internal receive data FIFO's or 0x24002 for a channel with an external receive data FIFO. Please note: the counts are LW based. x4 for byte counts.

Type 4 implementations require a wider count. The RX DMA FIFO is reported [only] in this register. The RX DDR FIFO CNT register has the full path with both DMA and IO FIFOs plus DDR and pipeline. The DMA count in this register is provided to allow for previous SW implementations to be used without modification. It is highly recommended to update to use the new count. The updated drivers return the correct version based on the design type.

The receive packet-length count field is also in this register. This allows the user to know how many packet-length values are stored in the packet-length FIFO. The first receive packet-length written to the packet-length FIFO is read as soon as it is written to be immediately available. This causes the receive packet-length valid status bit to be set, and the packet-length count to become one. As subsequent packets are received, the count will increment and as lengths are read, the count will decrement.

SPWR_CHAN_TX_PKT_LEN_0-3

[0x0064, 0x00B4, 0x0104, 0x0154] TX Packet length FIFO Ports (write only)

TX Packet Length FIFO Ports

Channels with 2 Gbyte Maximum Packet-Lengths

Data Bit	Description
31	Terminate Packet with an Error-End-of-Packet
30-0	Packet Length (31 bits)

FIGURE 18 SPACEWIRE TX PACKET LENGTH FIFO PORTS

SPWR_CHAN_RX_PKT_LEN_0-3

[0x0064, 0x00B4, 0x0104, 0x0154] RX Packet length FIFO Ports (read only)

RX Packet Length FIFO Ports

Channels with 2 Gbyte Maximum Packet-Lengths

Data Bit	Description
31	Connection Error or Error-End-of-Packet
30-0	Packet Length (31 bits)

FIGURE 19 SPACEWIRE RX PACKET LENGTH FIFO PORTS

These ports access the write transmit packet-length FIFO and the read receive packet-length FIFO ports for the respective channels. These FIFOs are used to store packet lengths for sending transmit packets and reading received packets.

The bit above the packet-length field is an error flag. If this bit is read as a one, it indicates that either the packet was terminated with an EEP (Error-End-of-Packet) or an error condition occurred while the packet was being received. If this bit is written as a one, it indicates that the transmit packet should be terminated with an EEP rather than an EOP.

SPWR_CHAN_TX_AMT_0-3

[0x0068, 0x00B8, 0x0108, 0x0158] TX Almost-Empty Level (read/write)

TX Almost Empty Level Register	
Data Bit	**Description**
31-0	TX FIFO Almost-Empty Level

FIGURE 20 SPACEWIRE CHANNEL TX ALMOST EMPTY LEVEL REGISTER

These read/write ports access the transmitter almost-empty level registers for the respective channels. When the number of data words in the transmit data FIFO is equal or less than this value, the almost empty status bit is set and an interrupt may be generated if it is enabled. While the port is defined larger than the FIFO size in LW, the comparison should be set to a value within the range of the FIFO for proper operation.

The value can be adjusted based on system requirements. There are separate HW [fixed] settings used to control data movement within the design. Alter to provide maximum OS delay time [larger value] or to minimize the number of transfers required [smaller value]. Use as a polled status bit or interrupt bit.

SPWR_CHAN_RX_AFL_0-3

[0x006C, 0x00BC, 0x010C, 0x015C] RX Almost-Full Level (read/write)

RX Almost Full Level Register	
Data Bit	**Description**
31-0	RX FIFO Almost-Full Level

FIGURE 21 SPACEWIRE CHANNEL RX ALMOST FULL LEVEL REGISTER

These read/write ports access the receiver almost-full level registers for the respective channels. When the number of data words in the receive data FIFO is equal or greater than this value, the almost full status bit is set and an interrupt may be generated if it is enabled. While the port is defined larger than the FIFO size in LW, the comparison should be set to a value within the range of the FIFO for proper operation.

SPWR_CHAN_CREDIT_AND_TIMECODE_STATUS_0-3

[0x0070, 0x00C0, 0x0110, 0x0160] Channel Credit and Time Code Status (read only)

Channel Credit and Timecode Status Register

Data Bit	Description
31	BurstOut Idle
30	BurstIn Idle
29	DDR Boundary Error Tx
28	DDR Boundary Error Rx
27-21	Spare
20	DMA SM Enabled
19-18	Spare
17-12	Channel Time Code
11-10	Spare
9-4	Transmit Credit
3	Spare
2-0	Flow Control Token Count

FIGURE 22 SPACEWIRE CHANNEL TIMECODE AND CREDIT STATUS REGISTER

Important note: This register was implemented for test and debug purposes only. Brief descriptions of each bit field are provided for reference. Detailed functional behavior is not provided as this register is not expected to be used in normal operation.

Flow Control Token Count: Current number of outstanding FCTs.

Transmit Credit: Number of characters channel is authorized to send - sync'd to PCI clock.

Channel Time Code: Timecode data into Channel – sync'd to PCI clock.

BurstOut and BurstIn Idle = '1' when in the idle state. '0' when busy.

DDR Boundary Error Tx and Rx = '1' when an error has occurred. The HW checks if the Stop address is less than the Start address. '0' is normal status.

DDR SM Enabled is '1' when the controller for the DDR is enabled. Read-back to make sure DDR is operating.

SPWR_CHAN_RX_PKT_FF_FULL_CNTRL_0-3

[0x0074, 0x00C4, 0x0114, 0x0164] RX Packet FIFO Full Control Register (read/write)

RX Packet FIFO Full Control Register

Data Bit	Description
31-10	Spare
9-0	RX Packet FIFO Full Level

FIGURE 23 SPACEWIRE CHANNEL RX PACKET FIFO FULL CONTROL REGISTER

These bits are set to 0x3DF on system power-up or reset.

RX Packet FIFO Full Level: These bits set the RX Packet FIFO Full Threshold level. By default these bits are set to 0x3DF. The RX Packet FIFO has 1024 locations (0x3FF) therefore, by default, the logic will see the FIFO as full once 960 or more locations are occupied, once the threshold is reached (or passed) the logic will back pressure the SpaceWire link by not providing additional FCT's until the number of FIFO locations drops below the threshold.

Per the SpaceWire specification the maximum outstanding FCTs is 56. If single byte transfers are being used and the maximum FCTs are outstanding when the FIFO goes full, 56 additional packets maybe received, 0x3DF was chosen to be the default value to cover this case.

Setting this register to either 0x3FF or 0x000 puts this logic in legacy mode. Other values can be used to retain protection and optimize for your system based on the minimum packet size [vs. FCTs].

SPWR_CHAN_TX_DDR_FIFO_CNT0-3

[0x28] TX Full path count Type 4 models(read only)

TX Word Count	
Data Bit	**Description**
31-0	Tx Word Count DDR

FIGURE 24 SPACEWIRE CHANNEL TX DDR FIFO COUNT

SPWR_CHAN_RX_DDR_FIFO_CNT0-3

[0x2C] RX Full path count Type 4 models(read only)

TX Word Count	
Data Bit	**Description**
31-0	Rx Word Count DDR

FIGURE 25 SPACEWIRE CHANNEL RX DDR FIFO COUNT

In a type 4 SpaceWire port [refer to figure 2] each Tx and Rx port have 2, 4K FIFOs implemented within the FPGA plus the DDR allocated external to the FPGA. The default setting is for 32 Mbytes DDR per Rx or Tx. The count returned includes the FIFOs, DDR acting like a FIFO and other minor storage to support DMA accesses etc. The max count is a function of how much memory is allocated to each port.

The original FIFO count register for Tx and Rx is modified to contain the DMA FIFO count for Rx and Tx IO count for the Tx version. Software can be left alone if desired. For better operation it is recommended to use these counts to make better use of the DDR.

SPWR_CHAN_BURSTIN_PTR0-3

[0x30] Tx DMA current address pointer Type 4 models(read only)

TX DMA Pointer	
Data Bit	**Description**
31-0	TX DMA current address

FIGURE 26 SPACEWIRE CHANNEL TX DDR CURRENT PTR

SPWR_CHAN_BURSTOUT_PTR0-3

[0x34] Rx DMA current address pointer Type 4 models(read only)

RX DMA Pointer	
Data Bit	**Description**
31-0	RX DMA current address

FIGURE 27 SPACEWIRE CHANNEL TX DDR CURRENT PTR

The pointers can be read to see where in the linked list the DMA engines are currently processing. Remember these are the direct HW addresses not the virtual addresses. Normally not used. Mainly used for debugging purposes.

SPWR_CHAN_TX_STRT_ADD0-3

[0x38] Tx Starting Address DDR Type 4 models(read only)

TX Start Address DDR	
Data Bit	**Description**
31-0	TX DDR Starting Address

FIGURE 28 SPACEWIRE CHANNEL TX DDR START ADDRESS

SPWR_CHAN_TX_STOP_ADD0-3

[0x3C] Tx Stop Address DDR Type 4 models(read only)

TX Stop Address DDR	
Data Bit	**Description**
31-0	TX DDR Stop Address

FIGURE 29 SPACEWIRE CHANNEL TX DDR STOP ADDRESS

SPWR_CHAN_RX_STRT_ADD0-3

[0x40] Rx Starting Address DDR Type 4 models(read only)

RX Start Address DDR	
Data Bit	**Description**
31-0	RX DDR Starting Address

FIGURE 30 SPACEWIRE CHANNEL RX DDR START ADDRESS

SPWR_CHAN_RX_STOP_ADD0-3

[0x44] Rx Stop Address DDR Type 4 models(read only)

TX Stop Address DDR	
Data Bit	**Description**
31-0	RX DDR Stop Address

FIGURE 31 SPACEWIRE CHANNEL RX DDR STOP ADDRESS

The start and stop addresses are used to create address spaces within the DDR memory. The registers within each port default to 8M LW or 32 Mbytes per space. The test menu prints out the contents of the registers and shows the total memory available.

The Start address and End address are included in the space.
Default:

Chan 0	RX DDR (0x0000000 – 0x1FFFFFC)	TX DDR (0x2000000 – 0x3FFFFFC)
Chan 1	RX DDR (0x4000000 – 0x5FFFFFE)	TX DDR (0x6000000 – 0x7FFFFFC)
Chan 2	RX DDR (0x8000000 – 0x9FFFFFC)	TX DDR (0xA000000 – 0xBFFFFFC)
Chan 3	RX DDR (0xC000000 – 0xDFFFFFC)	TX DDR (0xE000000 – 0xFFFFFFC)

In most cases the default allocation can be used. Should your project require more memory in one segment compared to another be careful not to overlap the address ranges and use byte addressing. HW converts to LW for counts and other uses. The DDR controller uses a byte address. The address is expected to be on a long word boundary[0,4,8,C]. It is recommended to line up with a page boundary for best performance. 1K address boundary.

HW handles refresh, arbitration etc. without software intervention required.

SpaceWire I/O Channel Pin Assignment

MDM Connectors

Channel 0

DIN 0 +	1	
DIN 0 -		6
SIN 0 +	2	
SIN 0 -		7
SHIELD0	3	
SOUT 0 +		8
SOUT 0 -	4	
DOUT 0 +		9
DOUT 0 -	5	

Channel 1

DIN 1 +	1	
DIN 1 -		6
SIN 1 +	2	
SIN 1 -		7
SHIELD1	3	
SOUT 1 +		8
SOUT 1 -	4	
DOUT 1 +		9
DOUT 1 -	5	

Channel 2

DIN 2 +	1	
DIN 2 -		6
SIN 2 +	2	
SIN 2 -		7
SHIELD2	3	
SOUT 2 +		8
SOUT 2 -	4	
DOUT 2 +		9
DOUT 2 -	5	

Channel 3

DIN 3 +	1	
DIN 3 -		6
SIN 3 +	2	
SIN 3 -		7
SHIELD3	3	
SOUT 3 +		8
SOUT 3 -	4	
DOUT 3 +		9
DOUT 3 -	5	

FIGURE 32 MDM I/O CONNECTOR PINOUTS

Channel #’s are consistent across boards.

(cc)PMC (PCI) Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the (cc)PMC-SpaceWire. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 33 (CC)PMC-SPACEWIRE PN1 INTERFACE

(cc)PMC (PCI) Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module Pn2 Interface on the (cc)PMC-SpaceWire. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
	+3.3V	11	12
RST#	BUSMODE3#	13	14
+3.3V	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24	+3.3V	23	24
IDSEL	AD23	25	26
+3.3V	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#	+3.3V	35	36
GND	STOP#	37	38
PERR#	GND	39	40
+3.3V	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8	+3.3V	49	50
AD7		51	52
+3.3V		53	54
	GND	55	56
		57	58
GND		59	60
	+3.3V	61	62
GND		63	64

FIGURE 34 (CC)PMC-SPACEWIRE PN2 INTERFACE

(cc)PMC Pn4 User Interface Pin Assignment

The figure below provides the pin assignments for the ccPMC and PMC SpaceWire Modules routed to Pn4. Also, see the User Manual for your carrier board for information on interfacing with Pn4. Ports 0-2 are only implemented on PMC Pn4 when the rear IO ordering option is selected.

DOUTA_0-	DINA_0-	1	2
DOUTA_0+	DINA_0+	3	4
GND REF		5	6
GND REF		7	8
SOUTA_0-	SINA_0-	9	10
SOUTA_0+	SINA_0+	11	12
		13	14
		15	16
DOUTA_1-	DINA_1-	17	18
DOUTA_1+	DINA_1+	19	20
GND REF		21	22
GND REF		23	24
SOUTA_1-	SINA_1-	25	26
SOUTA_1+	SINA_1+	27	28
		29	30
		31	32
DOUTA_2-	DINA_2-	33	34
DOUTA_2+	DINA_2+	35	36
GND REF		37	38
GND REF		39	40
SOUTA_2-	SINA_2-	41	42
SOUTA_2+	SINA_2+	43	44
		45	46
		47	48
DOUTA_3-	DINA_3-	49	50
DOUTA_3+	DINA_3+	51	52
GND REF		53	54
GND REF		55	56
SOUTA_3-	SINA_3-	57	58
SOUTA_3+	SINA_3+	59	60
		61	62
		63	64

FIGURE 35 (CC)PMC-SPACEWIRE PN4 INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-SpaceWire. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

Dynamic Engineering Modules are conceived and engineered for rugged industrial environments. The SpaceWire family is constructed out of 0.062-inch thick High-Temp ROHS compliant FR4 material.

ROHS and standard processing are available options.

Through-hole and surface-mount components are used. PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable. The PCI & PCIe gold fingers are gold over nickel for high reliability and long-lasting connections. PC104p stacking connectors are mounted in accordance with the manufacturers specifications and using gold plated mounting holes for reliable connections.

PMCs and ccPMCs are secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion for PMC. ccPMC has additional thermal rail mounting points which also enhance operation in high vibration environments. PC104p are stacked and retained with inter-module stand-offs and mounting hardware. PCI cards can be retained with bezel mount screws and internal card guides.

The PCB provides a (typical based on PMC) low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the board. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

The ccPMC version has internal thermal planes which are isolated from the electrical planes and tied to the thermal strips where the carrier conduction cooling webs are mounted. The exposed surfaces are gold plated for superior contact and thermal transfer with the web. The components are Industrial temperature rated or better. Thermal vias are added under components to tie in with the thermal plane directly.

The PC104p version of the design has the ground plane tied in with the mounting hardware to allow for inter-stack cooling in conduction cooled environments. Air cooling is also a viable method.

Thermal Considerations

The SpaceWire design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced-air cooling is recommended. With the one-degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options. https://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite B&C
Santa Cruz, CA 95060
831-457-8891
support@dyneng.com

Specifications

Formats:	ccPMC, PMC, PCI, PCIe, PC104p, PCI-104
Host Interface (PCI): Host Interface (PCIe)	PCI Interface 33 MHz. 32-bit PCIe 4 lane interface 1G.
Serial Interfaces:	Four SpaceWire channels
TX Bit-rates generated:	2 – 200 MHz for each SpaceWire channel
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	Long-word boundary space (see memory map)
Wait States:	One for all addresses
Interrupt:	Each channel has an interrupt for TX almost-empty, Rx almost-full, Time-code received, Rx packet done, and Rx error. Read and write DMA interrupts are also implemented for each channel.
DMA:	Independent input and output Scatter/Gather DMA Support implemented for each channel
Onboard Options:	All Options are Software Programmable
Interface Options (PMC):	Three 9-pin MDM connectors for channel 0 – 2, channel 3 available on Pn4 only. All channels can be strapped to interface with Pn4 only if desired

Interface Options (PCI/PCIe/PC104p): 9-pin MDM connectors for channel 0 – 4

Interface Options (ccPMC) Pn4

Dimensions (cc)PMC:	Standard Single (cc)PMC Module
Dimensions (PCI, PCIe):	Dimensions: 6.600 inches by 4.200 inches
Dimensions (PC104p)	Standard PC104p or PCI-104 card

Construction:	High Temp ROHS compliant FR4 Multi-Layer Printed Circuit, Through-Hole and Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC [similar for other formats]
Components	Industrial Temperature components standard
Power	3.3V and 5V. Both voltages +/- 5%

Order Information

Please refer to our SpaceWire webpage for the most up to date information:
https://www.dyneng.com/spacewire.html

PCIe-SpaceWire-BK	https://www.dyneng.com/PCIe-SpaceWire.html Standard version with two32 Mega-Byte FIFOs per channel, standard SpaceWire [ECSS-E-50-12C] timing and protocol. Four channels through the Bezel. Industrial Temperature STD. 200 MHz operation.
PCI-SpaceWire-BK	https://www.dyneng.com/pci_SpaceWire.html Standard version with two 64KB FIFOs per channel, standard SpaceWire [ECSS-E-50-12C] timing and protocol. Four channels through the Bezel. Industrial Temperature STD. 200 MHz operation.
PMC-SpaceWire-BK	https://www.dyneng.com/pmc_SpaceWire.html Standard version with two 32 Mega-Byte FIFOs per channel, standard SpaceWire [ECSS-E-50-12C] timing and protocol. Three channels through the Bezel, one at Pn4. Option for all at Pn4. Industrial Temperature STD. 200 MHz operation.
PC104p-SpaceWire-BK	https://www.dyneng.com/pc104p_SpaceWire.html Standard version with two 32 Mega-Byte FIFOs per channel, standard SpaceWire [ECSS-E-50-12C] timing and protocol. Four Ports. Industrial Temperature STD. 200 MHz operation.

Options:

-ROHS	Add ROHS compliant processing. Please note: Standard leaded processing will be used if this option is not selected.
-Pn4	Add for all channels through rear connector [Pn4] PMC model only
-CC	Add confomal coating. Quoted on a lot basis.
Software	Included for SpaceWire clients: Software Driver, sample application. Please specify Windows®, Linux. Onetime/project fee required for VxWorks.
MDM-SpaceWire	https://www.dyneng.com/SpaceWireCable.html 9-pin MDM connectors (2) - four shielded twisted pairs. Standard and custom lengths are available.
DESWBO	https://www.dyneng.com/deswbo.html Dynamic Engineering SpaceWire BreakOut [monitor / Debugger] with LED's for traffic status, headers to work with scope or analyzer for packet counts etc. Pass through configuration to monitor complete traffic between nodes.
DESWCB	https://www.dyneng.com/deswcb.html Dynamic Engineering SpaceWire Connector Board – multi-channel cable to single channel cable adapter. Up to 28 MDM connectors can be mounted – specify number when ordering – Plastic housing. Route multi-channel cable to side or rear of housing and break out in the front. Matched length traces, with strain relief for easy mounting of cable.