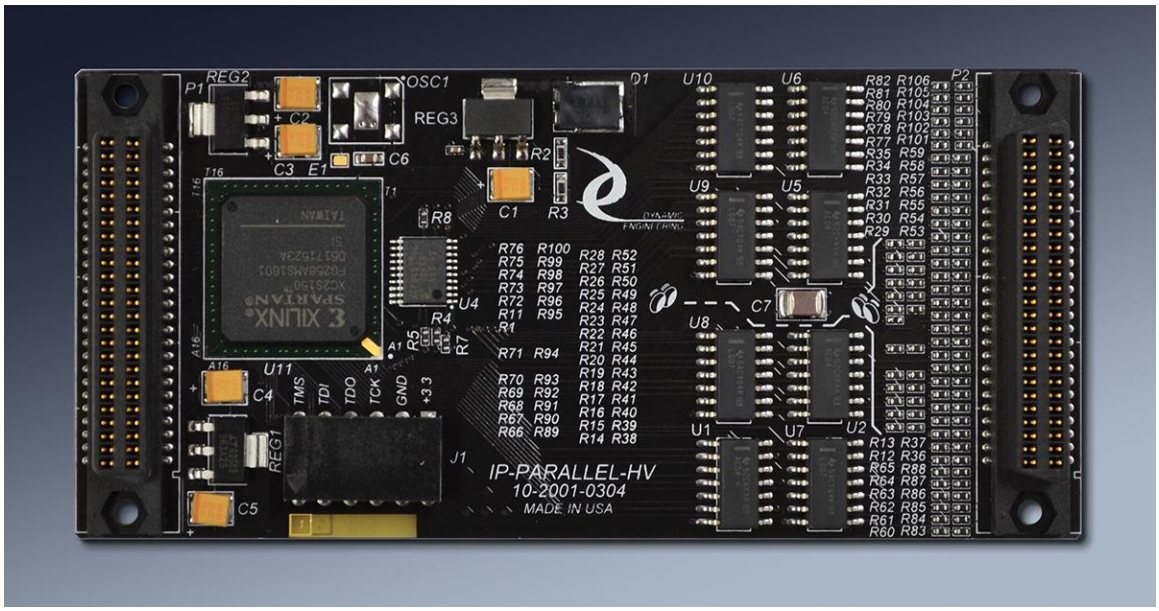
DYNAMIC ENGINEERING
150 DuBois St., Suite B&C Santa Cruz, CA 95060
(831) 457-8891
https://www.dyneng.com
sales@dyneng.com
Est. 1988

User Manual

IP-Parallel-HV

Digital Parallel Interface
IP Module
24 HV Outputs & Inputs



Revision 4 Shown

Revision 5p1 10/29/24
Corresponding Hardware: Revision 05

IP-Parallel-HV

Digital Parallel Interface
IP Module

Dynamic Engineering
150 DuBois St Suite B&C
Santa Cruz, CA 95060
www.dyneng.com

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

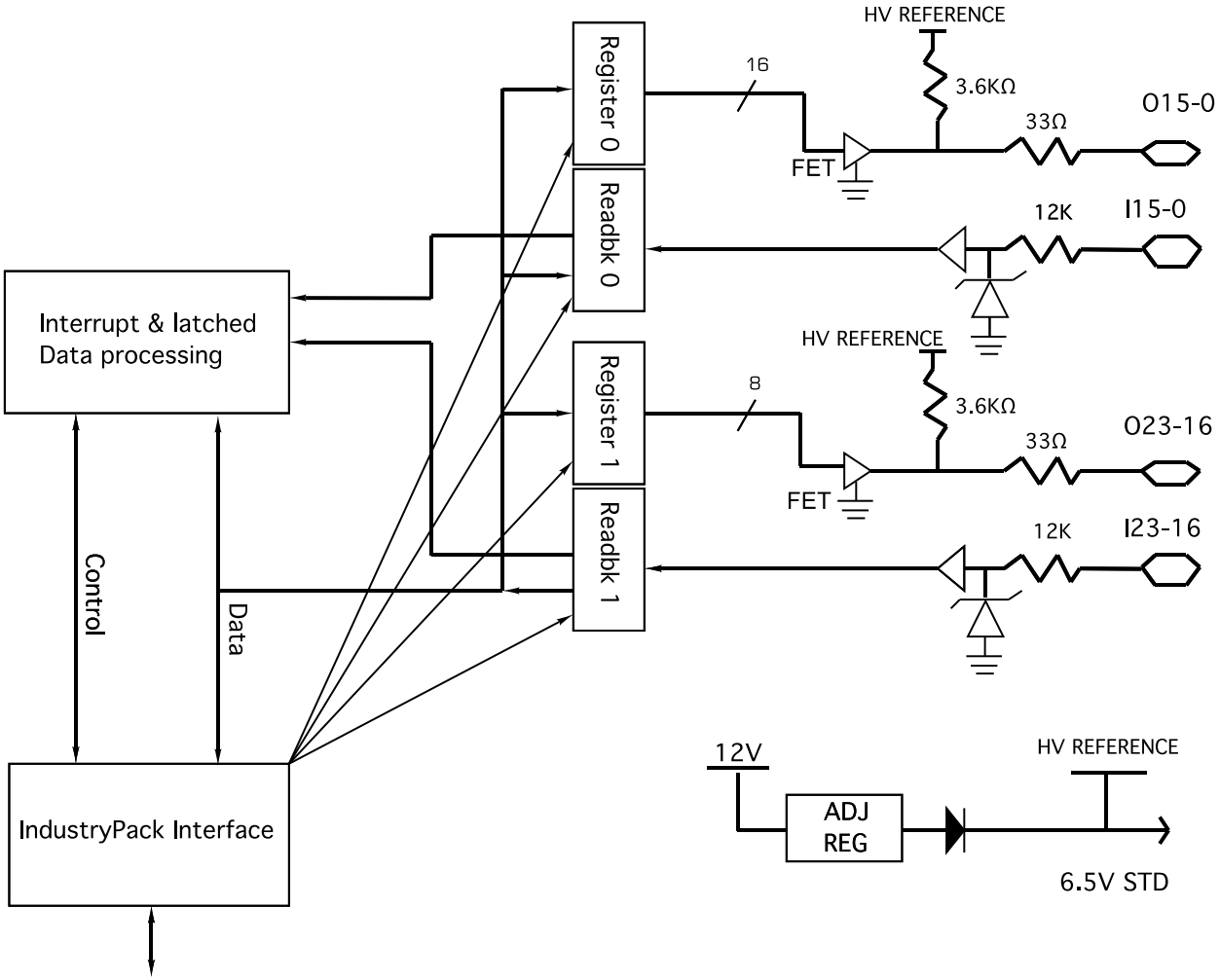
Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Table of Contents

List of Figures

Product Description and Operation



PCB Rev 5 Block Diagram. Previous versions had LS07 30V capable interface instead of the FETs with 50V and higher sink capability. Also Zener diodes were implemented with a voltage divider [39K].

IP-Parallel-HV is part of the IP Module family of modular I/O components. IP-Parallel-HV is capable of providing multiple protocols. The standard version provides 24 uncommitted outputs and 24 uncommitted inputs. With revision 5 PCB the outputs utilize FETs to provide a high voltage low side switch. The on-board regulator provides a 6.5V standard reference. Other on-board voltages can be supplied up to 12V. An external supply can be used when desired or if voltages above 12V need to be generated. Each input channel has a resistor divider to scale the input voltage back to "TTL" levels. The resistors can be altered for other voltage requirements. The external voltage has a range selector shunt to support higher voltages up to 50V.

With revision 5 PCB the Test and Standard versions have been merged. The Test version was basically the same and incorporated memory plus other features to allow full testing of Dynamic Engineering carriers. Most users will ignore these features. Please note the additions to the memory map. The IO definitions remain the same.

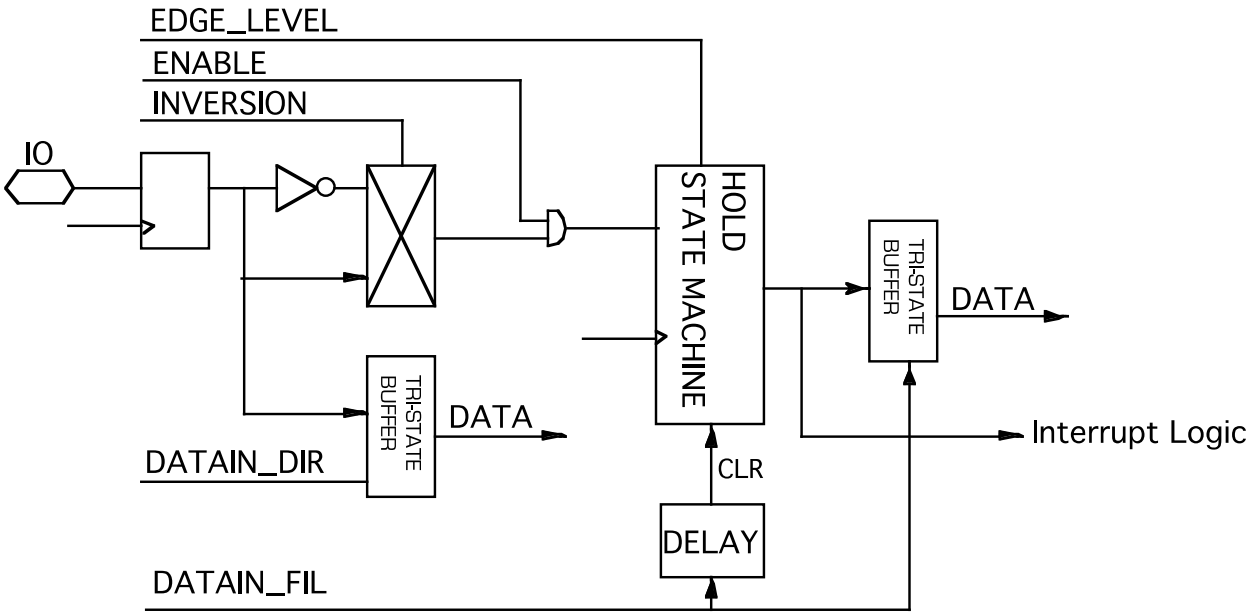
Each output channel has a register bit associated with it. When the register bit is set to '0' that channel turns on the FET and puts a '0' on the line. When the register bit is set to '1' then the FET is turned off and the pull-up will create a high level on the line unless some other system element is driving the line low. The register is read-write and will always return the value written to it. There are 24 output lines. 2 registers are dedicated to the output [23-0] bus.

The output bus is additionally supported by a control bit in the base control register. If the bit is disabled, then enabled after the control bits of interest are set into the output bus registers; all 24 outputs will be updated on the same clock edge. If left enabled then the outputs will be updated one clock after the register is updated. If disabled then the output control is held from the last enabled control setting. The reset default is FETs off.

Each Input line is also brought into the FPGA [Xilinx Spartan VI]. The input lines are available as a direct read or after filtering. The Input bits are independent of the Output bits. The inputs are received through buffers with hysteresis. The Signals are preconditioned by series 12K ohm resistor followed by a Zener diode to keep the voltage at the buffer within range. At maximum input level of 50V the Zener will shunt (50-3)/12K => 3.9 mA. Less at lower reference voltages.

Each Input channel has an enable, sense, and edge or level bit associated with it. The enable will block or enable a particular channel from being received into the filtered logic. The sense will either keep the current version or invert the data received. The edge or level control will make the hold circuit wait for an edge from 0 > 1 or react to a level. The hold circuit captures data and holds it until read. The data is registered at the chip edge and then again after the enable and inversion circuitry. Each channel has a separate hold circuit. If a signal is detected to be high then the signal is held until the

data is read. With the inversion capability each channel can be programmed to “be high” or to transition to a high condition when the channel has something of interest. The registers are referenced to the IP clock and operate at 8 or 32 MHz depending on the slot configuration. Each group of channels has a separate read clear signal. The channels can be read in any order and not loose data. The circuit will capture pulses down to 2 reference clocks wide. 60 nS or 250 nS with the standard IP reference clock.



The active high signals are combined to create an interrupt request based on the captured and held data. If the master interrupt enable is “enabled” then the interrupt is passed onto the system. The interrupt is cleared by reading the data or disabling the master enable. The user can program each channel to use the edge or level condition. The edge is particularly useful for long duration signal where repeated interrupts are not desired. The alternate approach is to flip the sense bit and create an interrupt when the signal has switched to the opposite polarity. Instruction order is important. Once the interrupt is detected the sense needs to be switched before the interrupt is re-enabled or a second interrupt is likely to be generated. It is recommended to read from the filtered data path after the processing parameters are changed to clear any interrupts that are created by the changing filter parameters.

With each Input line having all three controls a lot of control possibilities exist. If desired the Inputs can be tied to the Outputs for loop-back and bi-directional control.

In addition to the IO version, other custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there, we will redesign the state

machines and create a custom interface protocol. Please contact Dynamic Engineering with your custom application. There is a user oscillator position to support custom state machines and IO requirements. The DMA controls, second interrupt level, and memory space controls are routed to the FPGA to support the test modes and to allow for future upgrades.

IP-PARALLEL-HV supports both 8 and 32 Mhz. IP Bus operation. All configuration registers support read and write operations for maximum software convenience. Word operations are supported (please refer to the memory map). The Mem, ID, IO, and INT spaces are utilized by the IP-Parallel-HV (Test) design.

IP-PARALLEL-HV conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. PCI3IP and PCIe3IP make convenient development platforms in many cases.
https://www.dyneng.com/PCI3IP.html
https://www.dyneng.com/PCIe3IP.html

Interrupts are supported by IP-PARALLEL-HV. The interrupt occurs when a programmed transition occurs. The interrupts are individually maskable – each IO has a separate mask. The vector is user programmable by a read/write register. The interrupt occurs on IntReq0. The vector can be read in the IO space or automatically with the INT space.

Address Map

Function		Offset	Width	Type
DataOut0	EQU	$00	word	read/write
DataOut1	EQU	$02	word	read/write
BaseCntl	EQU	$06	word	read/write
Int En0	EQU	$08	word	read/write
Int En1	EQU	$0A	word	read/write
Vector	EQU	$0E	word	read/write
Int EdgLvl0	EQU	$10	word	read/write
Int EdgLvl1	EQU	$12	word	read/write
Int Pol0	EQU	$18	word	read/write
Int Pol1	EQU	$1A	word	read/write
IntStatus	EQU	$1E	word	read
dat_in_fil0	EQU	$20	word	read
dat_in_fil1	EQU	$22	word	read
dat_in_dir0	EQU	$28	word	read
dat_in_dir1	EQU	$2A	word	read
MemoryAddress	EQU	$2C	word	
IDPROM	byte on word boundary at ID offset			read
Memory Space	2Kx16 at Memory Offset.			R/W

FIGURE 1 IP-PARALLEL-HV INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-PARALLEL-HV. The addresses are all offsets from the select line [IDSEL, IOSEL, MEMSEL, INTSEL].

Programming

Programming IP-PARALLEL-HV requires only the ability to read and write data in the host's I/O space. The base addresses are determined by the IP Carrier board.

In order to receive data the software is only required to read from the "Direct" port. Alternatively the filtered data path can be programmed with the enable, Level and edge and then the Filtered data used. If desired, the interrupt can be enabled and the interrupt vector written to the vector register.

A typical sequence would be to first write to the vector register with the desired interrupt vector. Please note that some carrier boards are auto-vectored and do not use the interrupt vector. The interrupt service routine should be loaded and the mask should be set. The Level and Edge conditions programmed then the enables set to receive data. The incoming data can be pulsed. The hardware will hold any captured pulse or level detected until the data is read by the software.

Data is written to the DataOut registers. Any active low bits are used to enable the FETs. The drivers have ~200 mA sink capability [max] and overcome the pull-up to create a '0' on the bus. A '1' in a bit position turns off the FET leaving the pull-up to bring the level to a '1'. Other hardware in the system can also pull the signal line to '0'.

A 32 bit write/read will result in two 16 bit accesses to the hardware with automatic incrementing addresses. The 32 bit access is quite a bit faster than 2 x 16 bit accesses. Dynamic Engineering Carrier designs all feature auto conversion from 32 to 16 bit transfers. In addition, the PCIe based carriers support 64 bit accesses too. The lower 32 bits of the output, "data in filtered", and "data in direct", and memory can be used with 32 bit accesses.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

Register Definitions

DataOut0

$00 DataOut Register Port read/write

CONTROL REGISTER 0	
DATA BIT	**DESCRIPTION**
15-0	15-0 output data control bits

FIGURE 2 IP-PARALLEL-HV CONTROL REGISTER 0 BIT MAP

DataOut1

$02 DataOut Register Port read/write

CONTROL REGISTER 1	
DATA BIT	**DESCRIPTION**
15-8	spare
7-0	23-16 output data control bits

FIGURE 3 IP-PARALLEL-HV CONTROL REGISTER 1 BIT MAP

1. All bits are active low and are reset on power-up. Default to ‘FFFF’ off state.

Base_CNTL

$06 Base Control Register Port read/write

CONTROL REGISTER BASE	
DATA BIT	**DESCRIPTION**
15-4	spare
3	Force Interrupt Level 1
2	Force Interrupt Level 0
1	master interrupt enable 1 = enabled
0	Data Output Register Update Enable 1 = enabled

FIGURE 4 IP-PARALLEL-HV BASE CONTROL REGISTER BIT MAP

1. Data Output Register Update Enable is used to control when the Data Output register values are used to update the output registers. The registers are double buffered allowing the second [output] stage to be enabled / disabled for synchronization. If synchronization is needed set to '0' until both registers are written and then enable ['1']. The output bits will be driven to the new state at the same time. Referenced to the IP Clock. If the bit is left in the '1' state the Data outputs will change when the registers are independently updated.

2. INT_EN is the master interrupt enable. Default is 0. If set to 1 and one or more of the filtered input data conditions is met an interrupt will be generated on level 0.

3. Force Interrupt [0 & 1]is used to create an interrupt for test and software development purposes. Set the bit to cause an interrupt and clear the bit to remove the interrupt. The IO bits can be used for the same purpose if the filter controls are properly set. Requires INT_EN to be enabled.

INTerrupt Enable

Int_en0 $08 Interrupt Enable Control read/write

Interrupt Enable	
DATA BIT	**DESCRIPTION**
15-0	int_en 15-0 Interrupt Enable 1 = enabled, 0 = disabled

FIGURE 5 IP-PARALLEL-HV INTERRUPT ENABLE 0 BIT MAP

Int_en1 $0A Interrupt Enable Control read/write

Interrupt Enable	
DATA BIT	**DESCRIPTION**
15-8	spare
7-0	int_en 23-16 Interrupt Enable 1 = enabled, 0 = disabled

FIGURE 6 IP-PARALLEL-HV INTERRUPT ENABLE 1 BIT MAP

The data bits correspond to the Input lines. In the filtered path, if the control register bit is set to 1 the corresponding Input line is enabled to be a potential interrupter and captured by the hold circuit. The enable is applied after the inversion control.

INTerrupt Edge_Lvl

Edg_Lvl 0 $10 Interrupt Type Control read/write

EDGE_LVL	
DATA BIT	**DESCRIPTION**
15-0	Edg_Lvl 15-0 1 = edge, 0 = level

FIGURE 7 IP-PARALLEL-HV INTERRUPT EDG_LVL 0 BIT MAP

Edg_Lvl 1 $12 Interrupt Type Control read/write

EDGE_LVL	
DATA BIT	**DESCRIPTION**
15-8	spare
7-0	Edg_Lvl 23-16 1 = edge, 0 = level

FIGURE 8 IP-PARALLEL-HV INTERRUPT EDG_LVL 1 BIT MAP

The data bits correspond to the IO lines. In the filtered path, if the control register bit is set to 1 then the corresponding IO line is captured only if there is a transition from ‘0’ to ‘1’. If set to ‘0’ then anytime the IO line is detected to be ‘1’ the hold circuit will be set. The hold circuit will retain the data until read by the corresponding data_in_fi(x) is accessed. The hold circuits are after the enable and inversion in the pipeline.

INTerrupt Polarity

Pol 0 $18 Interrupt Polarity Control read/write

Polarity DATA BIT	DESCRIPTION
15-0	POL 15-0 1 = invert, 0 = not inverted

FIGURE 9 IP-PARALLEL-HV INTERRUPT POL 0 BIT MAP

Pol 1 $1A Interrupt Polarity Control read/write

Polarity DATA BIT	DESCRIPTION
15-8	spare
7-0	POL 23-16 1 = invert, 0 = not inverted

FIGURE 10 IP-PARALLEL-HV INTERRUPT POL 1 BIT MAP

The data bits correspond to the IO lines. In the filtered path if the control register bit is set to 1 then the corresponding IO line is inverted. If set to '0' then no inversion is applied. If set [inverted] and Edge Triggered the falling edge is used. If not set and Edge Triggered the rising edge is used. Similarly for the level option, if inverted the low state is used to create the interrupt.

Data Input Filtered

Datain_fil0 $20 Filtered Input Data read/write

Filtered Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_FIL 15-0

FIGURE 11 IP-PARALLEL-HV INTERRUPT DATAIN_FIL0 BIT MAP

Datain_fil1 $22 Filtered Input Data read/write

Filtered Data	
DATA BIT	**DESCRIPTION**
7-0	DATAIN_FIL 23-16

FIGURE 12 IP-PARALLEL-HV INTERRUPT DATAIN_FIL1 BIT MAP

The data bits correspond to the IO lines after the filters have been applied. The data remains latched until the register is read. The registers are independent for reading and clearing purposes. Read [clear] the registers after any control change to insure that no false positives are reported.

Data Input Direct

Datain_dir0 $28 Read Data Direct read/write

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	DATAIN_DIR 15-0

FIGURE 13 IP-PARALLEL-HV INTERRUPT DATAIN_DIR0 BIT MAP

Datain_dir1 $2A Read Data Direct read/write

Direct Data	
DATA BIT	**DESCRIPTION**
7-0	DATAIN_DIR 23-16

FIGURE 14 IP-PARALLEL-HV INTERRUPT DATAIN_DIR1 BIT MAP

The data bits correspond to the IO lines without filters being applied. The data is a direct reflection of the current state of the IO lines. Metastable protection registers are in place but no hold registers.

Memory Address Capture

MemoryAddress $2C Read stored address read only

Direct Data	
DATA BIT	**DESCRIPTION**
15-0	Address

FIGURE 14 IP-PARALLEL-HV STORED ADDRESS

When accessing the memory space the address field in the control bus is expanded. The A6-1 bits remain the same with the upper bits multiplexed onto the Data bits. A7 is driven on D0 etc. During a memory access this register captures the upper bits so they can be checked for operation. The test memory is 1Kx16 and not large enough to test the entire memory space.

VECTOR

$0E Interrupt Vector Port

The Interrupt vector for IP-Parallel-HV is stored in this byte wide register. This read/write register is initialized to ‘xxFF’ upon power-on reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered. The interrupt is automatically cleared when the CPU acknowledges the interrupt. If in an auto-vectored system [PCI, PCIe etc.] this register is not needed and can be used for BIT.

Interrupts

All IP Module interrupts support vectored operation. In VME and other vectored systems the vector from IP-PARALLEL-HV comes from a vector register loaded as part of the initialization process.

The IP-PARALLEL-HV state machines generate an interrupt request when a programmed condition is detected on the IO lines. The interrupt is mapped to interrupt request 0. If vectored the system will access the INT space. The hardware will automatically supply the appropriate interrupt vector. The source of the interrupt is obtained by reading DATA_IN_FIL0-1. The status remains valid until the registers are read. The interrupt status is auto-cleared when the registers are accessed.

Dynamic Engineering IP Module drivers do this in the ISR/DPR process and store the information for the user to retrieve in the ISR Status structure. In addition, Dynamic Engineering SW packages treat the interrupts as Auto-vectored using system resources to determine the source.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BASE_CNTL register. The individual enables for IO lines are controllable through INT_EN0-1. The enable operates before the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to read the holding register [DATAIN_FIL0-1], reset the board, or disable the interrupt. The Interrupt acknowledge cycle fetches the vector, but does not clear the interrupt request in this design.

If operating in a polled mode and making use of the interrupts for status the master interrupt should be disabled.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision to be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-PARALLEL-HV is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-Parallel-HV board will be recorded with a new code in the DRIVER ID and reserved fields.

Address	Data	HV
01	ASCII "I"	$49
03	ASCII "P"	$50
05	ASCII "A"	$41
07	ASCII "H"	$48
09	Manufacturer ID	$1E
0B	Model Number	$04
0D	Revision	$A0
0F	reserved	$00
11	Driver ID, low byte	$00
13	Driver ID, high byte	$00
15	No of extra bytes used	$2C
17	CRC	$68

FIGURE 15 IP-PARALLEL-HV ID PROM

External Voltages

IP-Parallel-HV has a regulator to create the reference to the Transmit IO. The regulator uses 12V and drops the reference to a programmed level with 6.5V the default. Alternate internal references are available by changing the feed-back resistors. A special PN will be created -XXV to support this option.

In addition, one of the IO pins is available for user supplied voltages up to 50V. The internal reference is isolated from the IO with a diode.

Note: With revision 5 the interface has been updated to use FETs for the output side and a series resistor with 3V Zener on the input side. With this configuration the reference voltage can be up to 50V. Revision 5 has an error limiting the output voltages. The input voltage range is the full 50V. IP-Test uses 6.5V for the reference. IP-Crypto and IP-Miller both use output voltages within the revision 5 linmitation. Revision 6 and later PCBs will have this limitation removed.

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-PARALLEL-HV. Pins marked n/c below are defined by the specification, but not used on the IP-PARALLEL-HV. Also see the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		DMAReq0*		5		30	
	D2		MEMSEL*		6		31
D3		DMAReq1*		7		32	
	D4		IntSel*		8		33
D5		DMAck*		9		34	
	D6		IOSel*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		DMAEnd*		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		IntReq0*		17		42	
	D14		A4		18		43
D15		IntReq1*		19		44	
	BS0*		A5		20		45
BS1*		n/c		21		46	
	n/c		A6		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		GND		25		50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 16 IP-PARALLEL-HV LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-PARALLEL-HV. Pins marked. Also see the User Manual for your carrier board for more information.

O_0		I_0		1		26	
	O_1		I_1		2		27
O_2		I_2		3		28	
	O_3		I_3		4		29
O_4		I_4		5		30	
	O_5		I_5		6		31
O_6		I_6		7		32	
	O_7		I_7		8		33
O_8		I_8		9		34	
	O_9		I_9		10		35
O_10		I_10		11		36	
	O_11		I_11		12		37
O_12		I_12		13		38	
	O_13		I_13		14		39
O_14		I_14		15		40	
	O_15		I_15		16		41
O_16		I_16		17		42	
	O_17		I_17		18		43
O_18		I_18		19		44	
	O_19		I_19		20		45
O_20		IO_20		21		46	
	O_21		I_21		22		47
O_22		I_22		23		48	
	O_23		I_23		24		49
VIO		GND		25		50	

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 17 IP-PARALLEL-HV IO INTERFACE

“O” 23-0 Correspond to the output signals and map directly from DataOutput.
“I” 23-0 Correspond to the input signals and map directly to the direct and filtered data paths.

VIO is used to source 6.5V in this design. Diode protection allows external voltages to be connected to IP-Parallel-HV. The external voltage must be greater than the reference voltage to take effect. With changes to the regulator settings [resistors] the onboard regulator can be “programmed” for other reference voltages [12 V max output]

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the IP-Parallel-HV when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. The open collector drivers can handle relatively large offsets in voltage and are designed to operate when parts of the system are powered and parts are not. The IP-Parallel-HV does not contain special input protection other than the resistor divider. It is better design practice to keep the voltage offsets minimized and the potential for current flowing though un-powered electronics to a minimum.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [https://www.dyneng.com/HDRterm50.html] Dynamic Engineering also stocks ribbon cable in a variety of lengths. https://www.dyneng.com/HDRribn50.html

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

Loop-back Connections

The ATP software we use to test the IP-Parallel-HV includes a loop-back test. The Engineering Kit for the IP-Parallel-HV includes the source code for the ATP. The loop-back test is facilitated with an IP-Debug-IO card with added wire-wrapped interconnections.

Model “HV”

From	To	Signal
49	24	I23 – O23
48	23	I22 – O22
47	22	I21 – O21
46	21	I20 – O20
45	20	I19 – O19
44	19	I18 – O18
43	18	I17 – O17
42	17	I16 – O16
41	16	I15 – O15
40	15	I14 – O14
39	14	I13 – O13
38	13	I12 – O12
37	12	I11 – O11
36	11	I10 – O10
35	10	I9 – O9
34	9	I8 – O8
33	8	I7 - O7
32	7	I6 - O6
31	6	I5 - O5
30	5	I4 - O4
29	4	I3 - O3
28	3	I2 - O2
27	2	I1 - O1
26	1	I0 - O0

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-PARALLEL-HV is constructed out of high temperature ROHS compliant 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required. *Please order standard mounting kit for IPs if you want this option*. [IP-MTG-KIT]

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-Parallel-HV design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
https://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite B&C
Santa Cruz, CA 95060
831-457-8891
support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Parallel Interface:	24 open collector outputs. 200 mA sink with 3.6KΩ pull-up to reference Voltage. 24 Inputs with resistor / diode divider. Standard reference voltage of 6.5V
Software Interface:	Control Registers, ID PROM, Vector Register, Status Ports
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	Word I/O Space (see memory map) Word in ID Space Vectored interrupt Word, Byte in memory space
Access Time:	back-to-back cycles in 500ns (8Mhz.) or 125 nS (32 Mhz.)
Wait States:	1 to all spaces
Interrupt:	Multiple interrupt filtering options available on each IO line. Enabled, Active hi or low, edge or level.
DMA:	No Logic Interface DMA Support implemented at this time.
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface [HDRterm50] User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	High temp ROHS compliant FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{O}C for uniform heat across IP
Power:	Max. **TBD** mA @ 5
MTBF	1.855 M Hours GB 25C Bellcore

Order Information

The IP-Parallel-HV https://www.dyneng.com/ip_parallel_hv.shtml

"**HV"**	IP Module with 48 HV IO 24 FETs with pull-up [3.6K to VCCA] – other values available. 24 Inputs with 12K series with 3V Zener to ground. VCCA up to 50V. Internal VCCA up to 12V, 6.5V STD.

Tools for IP-PARALLEL-HV

IP-Debug-Bus	IP Bus interface extender with testpoints, isolated power and quick switch technology to allow hot swapping of IPs or power cycling without powering down the host. https://www.dyneng.com/ipdbgbus.html
IP-Debug-IO	IndustryPack IO connector breakout with test points, ribbon cable headers, and locations for user circuits. https://www.dyneng.com/ipdbgio.html
HDRterm50	Ribbon cable compatible 50 pin header to 50 screw terminal header. DIN rail mounting option. https://www.dyneng.com/HDRterm50.html
IP-MTG-KIT	4 metric stainless screw and stand-off pairs to retain IP-Parallel-HV against the carrier board. Flat head screws match IP Specification mounting requirements.