



DYNAMIC ENGINEERING

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Est. 1988

Statement of Volatility

PN: ccXMC-Serial

Manufacturer Part Number: ccXMC-Serial, includes all types (-HDLC, etc.)

Manufacturer Part Description: Conduction Cooled XMC with FPGA, DDR options, RS485 and LVDS options, RS-232/RS-485 IO, rear IO, PLL

Memory Type: FLASH, SRAM, DDR

Memory Size: varies with installed FPGA and DDR

Volatility: SRAM and DDR memories cleared by power cycle. FLASH is retained through power cycle. FLASH is not accessible by user for writing or read-back. FLASH is used to reload FPGA at power-on.

User Accessible: SRAM within FPGA is configured into registers etc. FPGA features are R/W [in many cases] to user software. SRAM contents are lost at power down and re-written with base design from FLASH upon power-on. DDR is used to store user data during operation. All data is lost when powered down. When reset, pointers are reset making current data inaccessible. Some models do not utilize DDR memory.

Clearing Procedure: Power cycle or re-write data stored contents per approved procedure. SRAM model for internal and FIFO.

Notes or Warnings: None