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Est. 1988

User Manual

PMC BiSerial-II NVY1

Bi-directional Serial Data Interface PMC Module

Revision B
Corresponding Hardware: Revision A
10-2002-1201

PMC BiSerial-II NVY1
Bi-Directional Serial Data Interface
PMC Module

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Manual Revision B. Revised June 9, 2003.

Table of Contents

List of Figures

Product Description

The PMC BiSerial-II NVY1 is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC BiSerial-II is capable of providing multiple serial protocols. The NVY1 protocol implemented provides Manchester encoded data inputs and outputs.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a "standard" special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

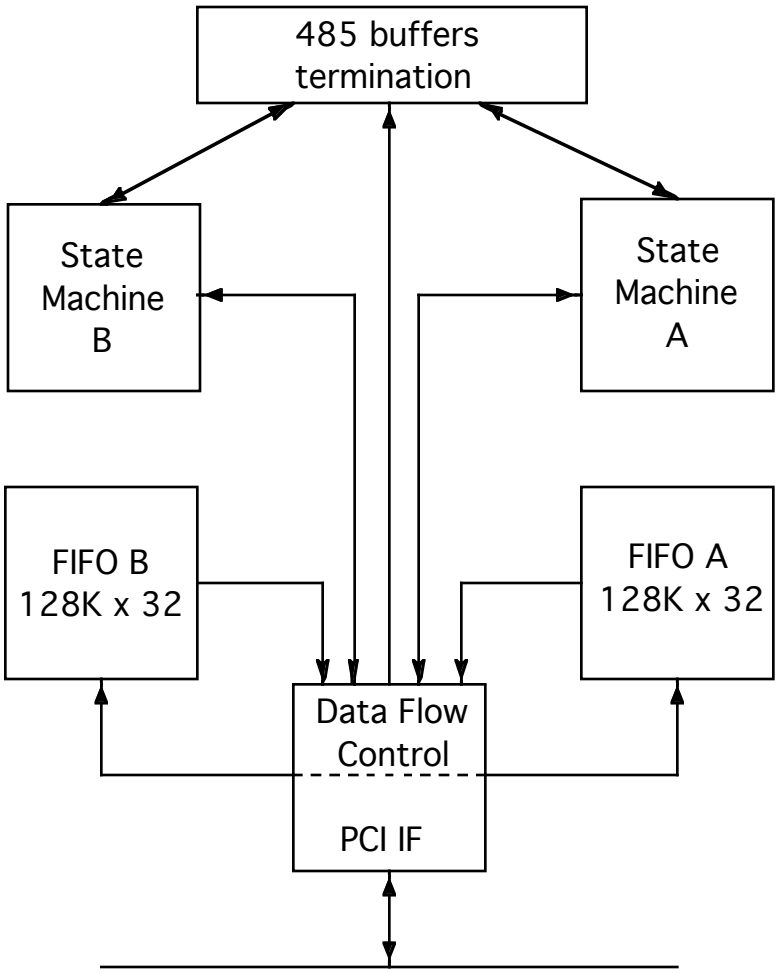

FIGURE 1 PMC BISERIAL-II BLOCK DIAGRAM

The transmit data rate is derived from the 62.208 MHz on-board oscillator. The normal transmitter data rate is 10.368 MHz (divide-by 6), but divide-by 4, 8, 10, 12, 14, and 16 are also provided. The receiver automatically adjusts to data

rates that range from divide-by 5 to divide-by 12 of the 62.208 MHz oscillator (5.2 to 12.4 MHz).

The FIFOs always operate at the PCI clock frequency of 33 MHz to simplify testing and operational functions.

Thirty-two differential I/O are provided for the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 100Ω. The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pullup/pulldown resistor packs can also be installed to provide a logic '1' on undriven lines. The terminations and transceivers are programmable through the Xilinx device to provide the proper mix of outputs and inputs and terminations needed for a specific protocol implementation.

All configuration registers support read and write operations for maximum software convenience, and all addresses are long word aligned.

The PMC BiSerial-II conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

The PMC BiSerial-II uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors [height] to mate with the PMC BiSerial-II, please let us know. We may be able to do a special build with a different height connector to compensate.

The serial channels are each supported by a 128K by 32-bit FIFO. The FIFOs support long word reads and writes. A full 32-bit path exists for loop-back testing of each FIFO. Data is latched and the bus immediately released on a write-cycle. As soon as data is present in the FIFO it is pre-read to be immediately available for a read cycle. This allows minimal delay on the PCI write to TX FIFO path and PCI read from the RX FIFO path as well as access for the Tx and Rx state machines.

The serial receive channels can receive continuous or burst data in two paired data streams. As each pair of 16-bit words is received, the data is concatenated into a 32-bit word and stored in the Receive FIFO. The host can poll the FIFO flags or wait for the programmable FIFO Almost Full flag interrupt. The message can then be read over the PCI bus directly from the FIFO.

The Output channel has a separate 128K x 32-bit FIFO. The FIFO is written as long words, but the transmitter can be configured to send the entire 32 bits or the lowest 1, 2, or 3 bytes, msb first. If no data is in the FIFO, and the transmitter is not disabled, a hex 53 will be sent at a regular interval. This

interval will have a minimum of 1152 bit periods and a maximum of 65536 bit periods. The intervening bits will contain the 2-bit idle pattern specified in the Tx control register. If data is written to the FIFO during this process, the FIFO data will be sent out instead of the hex 53 pattern when the next time slot occurs. After the FIFO data is exhausted the hex 53 pattern will resume, maintaining the same time interval.

Various interrupts are supported by the PMC BiSerial-II NVY1. An interrupt can be configured to occur at the end of a transmitted message. In addition to this protocol interrupt there are interrupts associated with the programmable FIFO flags, the acquisition and loss of sync lock, the detection of each sync word, and the detection of incoherent clocks on the receiver. All interrupts are individually maskable and a master interrupt enable is also provided to disable all interrupts simultaneously. The current status is available for the FIFOs making it possible to operate in a polled mode. The Programmable Almost Full flag can be used with the receive channel to allow user software to read data from the FIFO on an interrupt basis with long messages [longer than the 128K of FIFO]. The Programmable Almost Empty flag is used with the transmitter to allow software to operate in an interrupt driven mode and to keep the TX FIFO from going empty. There are also four interrupts associated with the UART channel: Tx done, Rx data available, Parity error detected, and Framing error detected.

Theory of Operation

The PMC BiSerial-II NVY1 is designed for transferring data from one point to another with a Manchester encoded serial protocol.

The PMC BiSerial-II NVY1 features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BiSerial II design. Only the transceivers, switches, and FIFO's are external to the Xilinx device.

The PMC BiSerial-II is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. In standard configuration, the PMC BiSerial-II is a Type 1 mechanical with no components on the back of the board and one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

The PCI interface to the host CPU is controlled by a logic block within the Xilinx. The BiSerial II design requires one wait state for read or write cycles to any address. The PMC BiSerial-II is capable of supporting 40 MBytes per second into and out of the FIFO's. The wait states refer to the number of clocks after the PCI core decode before the "terminate with data" state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate with data state into the TRDY signal.

The BiSerial II can support many protocols. The PMC BiSerial-II NVY1 uses Manchester encoded data where clock and data information are sent on one serial link. At least one transition occurs in each bit period allowing the clock to be recovered from the data stream. The timing is shown in the next diagram.

A pair of state machines within the FPGA control all transfers between the FIFO and FPGA, and the FPGA and the data buffers. The TX state machine reads from the transmit FIFOs and loads the shift registers before sending the data. The RX state machine receives data from the data buffers and takes care of moving data from the shift register into the RX FIFO.

Data is read from the TX FIFO and loaded into the shift register. The MSB is then present at the output of the data buffer. One half-bit period later the data value is inverted to encode the clock on the data stream. One half-bit period later, the data is transitioned to the next value. The MSB-1 is now on the data lines. This process repeats until the first word is transferred. If more data is available from the FIFO, then the process repeats for the second word. In the standard timing there are no inter-word gaps, the data stream is continuous from MSB to LSB for a compact serial transfer. The data rate is set by a 3-bit field in the Tx control register, if these bits are all zero the default is divide-by six, or 10.368 MHz. Please refer to the register bit definitions for more details.

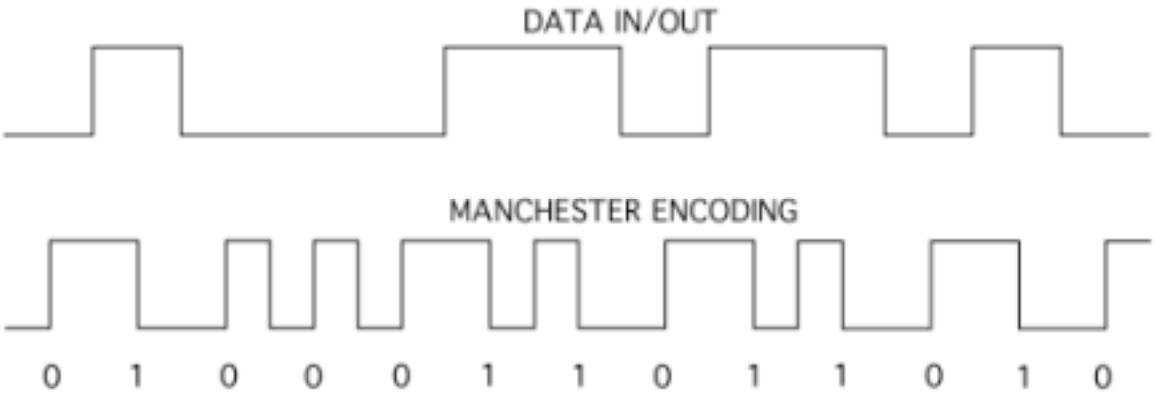

FIGURE 2 MANCHESTER DATA ENCODING

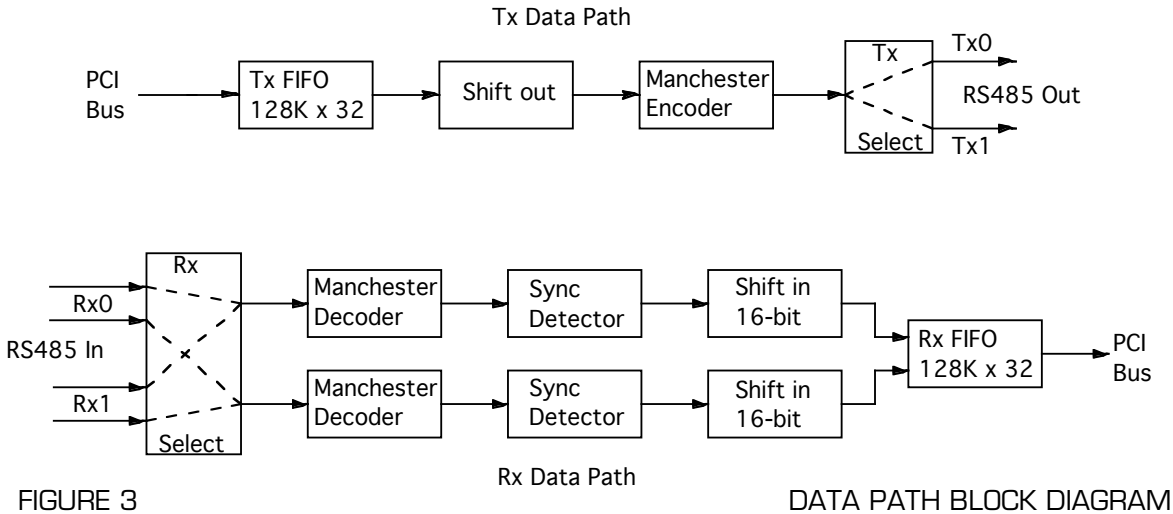

FIGURE 3 DATA PATH BLOCK DIAGRAM

The receive function is more complex. The data is received in two separate streams, assumed to be synchronized with each other. When the receiver is enabled the Manchester decoding circuit attempts to lock onto the proper bit period. Once a transition occurs in the data from a one to a zero or a zero to a one the decoder can distinguish between the mid-period transitions that encode the clock and the inter-period transitions that may or may not be present depending on the data pattern. The Manchester decoder recovers the clock from the data and the data proceeds to the sync detection circuit.

The sync detector searches for one of two 48-bit sync patterns and, if the pattern is found, inserts a four bit flag into the data stream replacing the four most significant bits in the third 16-bit word following the sync pattern. Once the sync pattern is found the alignment of the 16-bit words is determined. The two data streams are concatenated into one 32-bit wide data stream, and the data is

stored in the FIFOs. A simplified block diagram of the TX and RX paths is shown in the figure above.

Address Map

REGISTER		OFFSET	FUNCTION	TYPE
BIS2_BASE	EQU	$00	Base control register	read/write
BIS2_INTEN	EQU	$04	Interrupt enables	read/write
BIS2_TX	EQU	$08	Transmit control	read/write
BIS2_RX	EQU	$0C	Receive control	read/write
BIS2_UART	EQU	$10	UART control	read/write
BIS2_STAT0	EQU	$14	Status register 0	read
BIS2_SW_IN	EQU	$18	User switch port	read
BIS2_STAT1	EQU	$1C	Latched interrupt bits	read/write
BIS2_FIFOTX	EQU	$20	Transmit FIFO access	read/write
BIS2_FIFORX	EQU	$24	Receive FIFO access	read/write
BIS2_DIR_TERM	EQU	$28	Direction & termination bits	read/write
BIS2_SYNCW1H	EQU	$2C	Sync word 1 - 24 upper bits	read/write
BIS2_SYNCW1L	EQU	$30	Sync word 1 - 24 lower bits	read/write
BIS2_SYNCW2H	EQU	$34	Sync word 2 - 24 upper bits	read/write
BIS2_SYNCW2L	EQU	$38	Sync word 2 - 24 lower bits	read/write
BIS2_UART_DATA	EQU	$3C	UART Tx/Rx data	read/write

FIGURE 4 PMC BISERIAL-II INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the PMC BiSerial-II. The addresses are all offsets from a base address, which is assigned by the system when the PCI bus is configured.

The VendorId = 0x10EE. The CardId = 0x0014. Current revision = 0x01

Programming

Programming the PMC BiSerial-II NVY1 requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC BiSerial-II "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to receive data the software is only required to enable the Rx FIFO, Rx state machine, load the sync word values, sync options, store options, and scan length. Depending on these values, and the sync pattern received data may be loaded into the FIFOs. If no values are entered for the sync words, they default to 0x46afd1fc86f2 for the ping sync (sync word 1) and 0xb9af2efc86f2 for the scan sync (sync word 2). The scan length defaults to 864 bit periods.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the acquisition or loss of sync lock or the programmable almost full or empty interrupts, or the FIFO empty flag can be polled to indicate data is present In the FIFO. After the interrupt is received, the data can be retrieved. An efficient loop can then be implemented to fetch the data. New messages can be received even as the current one is read from the FIFO. If the FIFO throttle bit is set, the Rx state machine will stop storing data when the FIFO becomes almost full and won't start storing again until the FIFO is almost empty.

The TX interrupt indicates to the software that a message has been sent and that the message has completed. If more than one interrupt is enabled, then the SW needs to read BIS2_STAT1 to see which source caused the interrupt. The status bits of BIS2_STAT1 are latched and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

Whenever enabled and the FIFO is empty, the transmitter will automatically send a 0x53 command repeatedly at a regular interval that can be programmed with the Tx control register. Whenever data is written to the FIFO, this data will be sent in place of the 0x53 maintaining the same timing interval specified. When the FIFO becomes empty, the Tx interrupt will be set and the transmitted data reverts to the 0x53 data pattern with the same interval between messages. The only way to stop the transmitter is to set the Tx disable bit in the Tx control register.

Messages longer than 128K words can be accommodated by polling or using the

programmable flag interrupts. To poll, read the Status 0 register during the transfer and take appropriate action. The full, empty or programmable flags show that there is data to read or space to write. The PAE and PAF flags are implemented to provide an almost empty interrupt to allow the TX side to operate in an interrupt driven mode with longer messages. Similarly, the PAF can be used to provide an almost full interrupt for the receive side to allow interrupt driven long message capability.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

Register Definitions

BIS2_BASE

[$00] BiSerial II Base Control Register Port read/write

CONTROL BASE	
DATA BIT	DESCRIPTION
31-12	Spare
11	1 = Unit 5 selected, 0 = Unit 4 selected
10-8	Clock divisor, Freq = 62.208/(2*(n+1)), n>0
7	Spare
6	Spare
5	1 = Load B almost levels, 0 = Data accesses
4	1 = FIFO B enabled, 0 = FIFO B reset
3	1 = Load A almost levels, 0 = Data accesses
2	1 = User Switch Enabled, 0 = Normal
1	Spare
0	1 = FIFO A enabled, 0 = FIFO A reset

FIGURE 5 PMC BISERIAL-II BASE CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

Unit select is used to select the active unit that is communicating with the board. When this bit is a zero unit 4 is selected (Tx: I04, Rx: I012 &13, UART: Tx – I07, Rx – I018); when unit select is a one, unit 5 is selected(TX: I05, Rx: I014 & 15, UART: Tx – I06, Rx – I016).

Clock divisor determines the data rate of the transmitter. If this value is zero the divisor n defaults to 2 (divide-by 6) otherwise the bit rate is determined by the following formula. Rate = 62.208 MHz / (2 * (n + 1))

Load A Load B controls the loading and reading of the almost full/empty flag levels. When this bit is a one, FIFO read/write accesses are redirected to the level registers in sequential order Almost Empty, Almost Full, Almost Empty etc. When zero, normal data accesses are enabled. The level of this signal when the respective FIFO is reset determines the default levels at which the almost full/empty signals operate and the method used to reprogram these levels. If Load is high when reset is asserted, parallel programming is enabled and the default offset is 4095 words, if low, serial programming is enabled and the default offset is 255 words, serial programming of the almost full/empty flags is not supported by this hardware.

Note: In order to read the FIFO almost full/empty flag values, write two data values into the respective FIFO first. The data is pre-read from the FIFO and further reads will not be done if the FIFO is empty. Then set the Load bit high and read the flag levels. The first value returned will be a data value, so ignore it. The next is the almost empty and then the almost full. Now set the Load bit low again and do one more data read to purge the pre-read register. Writing these flag level registers does not require a special process, just set the Load high and write the two values.

Enable A Enable B enables and resets the FIFO. When this bit goes low the FIFO is reset and when it is one the FIFO is enabled. A reset sequence should be performed after power up before FIFO writes can take place.

User switch enable gates the user dip-switch value onto the lower eight data lines for FIFO A when this bit is a one. A zero value enables normal FIFO access.

BIS2_INTEN

[$04] BiSerial II Interrupt Enable Register Port read/write

CONTROL INTERRUPT ENABLE

DATA BIT	DESCRIPTION
31-18	Spare
17	Master Interrupt Enable
16	Force Interrupt
15	Spare
14	Spare
13	Tx done int enable
12	Sync lost lock int enable
11	Sync lock acquired int enable
10	Cock error int enable
9	High Sync detect int enable
8	Low Sync detect int enable
7	UART parity error int enable
6	UART frame error int enable
5	UART data available int enable
4	UART transmit done int enable
3	FIFO B almost full int enable
2	FIFO B almost empty int enable
1	FIFO A almost full int enable
0	FIFO A almost empty int enable

FIGURE 6 PMC BISERIAL-II INTERRUPT ENABLE REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

Master Interrupt Enable must be set to a one in order to cause a system interrupt when an enabled interrupt condition occurs. When this bit is zero, all interrupts are disabled.

Force Interrupt causes a system interrupt when set to a one if Master Interrupt Enable is asserted. This bit is used to test interrupt processing.

Tx done int enable when set to a one, enables the Tx done interrupt. This interrupt occurs when a transmit message completes.

Sync lost lock int enable when set to a one, enables the sync lost interrupt. This occurs when sync lock is acquired and then lost.

Sync lock acquired int enable when set to a one, enables the sync lock acquired interrupt. This occurs when three successive sync words are detected with the proper scan length between them.

Cock error int enable when set to a one, enables the clock error interrupt. This occurs when the high and low clock strobes are not coherent.

High Sync detect int enable when set to a one, enables the high sync detected interrupt. This occurs whenever a sync word is detected on the upper Rx link.

Low Sync detect int enable when set to a one, enables the low sync detected interrupt. This occurs whenever a sync word is detected on the lower Rx link.

UART parity error int enable when set to a one, enables the UART parity error detected interrupt. This occurs when the parity bit sent does not match the parity calculated by the UART receiver.

UART frame error int enable when set to a one, enables the UART framing error detected interrupt. This occurs when the receiver level is not high when the stop bit should be being received.

UART data available int enable when set to a one, enables the UART data available interrupt. This occurs when a character is received by the UART receiver.

UART transmit done int enable when set to a one, enables the UART transmit done interrupt. This occurs when a character transmission completes.

FIFO B almost full int enable when set to a one, enables the FIFO B almost full interrupt. This occurs when FIFO B becomes almost full as defined by the FIFO almost full flag register.

FIFO B almost empty int enable when set to a one, enables the FIFO B almost empty interrupt. This occurs when FIFO B becomes almost empty as defined by the FIFO almost empty flag register.

FIFO A almost full int enable when set to a one, enables the FIFO A almost full interrupt. This occurs when FIFO A becomes almost full as defined by the FIFO almost full flag register.

FIFO A almost empty int enable when set to a one, enables the FIFO A almost empty interrupt. This occurs when FIFO A becomes almost empty as defined by the FIFO almost empty flag register.

BIS2_TX

[$08] BiSerial II Tx Control Register Port read/write

CONTROL TX

DATA BIT	DESCRIPTION
31-24	Spare
23-8	Tx Delay
7-6	Tx Idle
5-4	Tx Size
3	Tx Test
2	FIFO Loop Test A
1	Tx Invert
0	Tx Disable

FIGURE 7 PMC BISERIAL-II TX CONTROL REGISTER BIT MAP

Tx Delay determines the interval at which the Tx commands are sent. If this value is less than the minimum interval (1152) then the minimum will be used, otherwise the interval = TxDelay+1 Tx bit periods. This interval is measured from the start of one message to the start of the next.

Tx Idle specifies the two-bit pattern that is sent whenever actual data is not being sent.

Tx Size determines the number of bytes sent from each FIFO word. If this field is "00" then one byte is sent, if "01" two bytes are sent, if "10" three bytes are sent, and if "11" all four bytes are sent.

Tx Test when set to a one enables both Tx outputs simultaneously. This is used for testing of the dual receiver lines.

FIFO Loop Test A when set to a one allows both reading and writing of FIFO A from the PCI bus. This is used to test the FIFO.

Tx Invert when set to a one inverts the logic levels of the transmitted data.

Tx Disable when set to a one disables the transmission of both FIFO data and the automatic 0x53 command.

BIS2_RX

[$0C] BiSerial II Rx Control Register Port read/write

CONTROL RX	
DATA BIT	DESCRIPTION
31-24	Spare
23-12	Scan Sequence Length
11	Spare
10-9	Store Options
8	Lock Status Source
7-6	Sync Options
5	Skip Scan Syncs
4	Skip Ping Syncs
3	FIFO Throttle Enable
2	FIFO Loop Test B
1	Rx Invert
0	Rx Enable

FIGURE 8 PMC BISERIAL-II RX CONTROL REGISTER BIT MAP

Scan Sequence Length specifies the number of bits in a single scan frame. This is measured from the beginning of one sync word to the beginning of the next sync word and is used as an error check. When a sync word is detected, the circuit expects to see another sync after this number of bits have been received.

Store Options determines when data is stored in the FIFO's. If bit 9 is a one, data is stored before sync is detected, when a valid sync is seen the data is aligned to the sync word and data continues to be stored. If bit 9 is a zero, no data is stored before the first sync is seen. If bit 10 is a one, data is not stored between the first sync and sync lock (three consecutive sync words detected). Therefore, if this field is "01" all data is stored, if "00" data is stored only after a sync is seen and if "10" no data is stored until sync lock is achieved. If "11" is selected all data will be stored except between the first sync detected and the sync lock state, this is probably not very useful, but is a valid option.

Lock Status Source determines the source for the lock status bit and the lock acquisition and loss interrupts. If this bit is a zero, the lock status will be '1' if either data stream is in a locked state. If this bit is one, both data streams must be locked before the lock status is true. The operation is not affected by this choice except by the effects of an interrupt occurring when the lock status changes.

Sync Options determines how the sync detection is coordinated in the two data streams. If this field is "00" the sync detectors operate independently, if "01" a sync seen by either stream will be detected by both, if "10" a sync must be seen simultaneously in both data streams to be detected, and if "11" no syncs are detected.

Skip Scan Syncs when set to a one causes scan sync words to be ignored.

Skip Ping Syncs when set to a one causes ping sync words to be ignored.

FIFO Throttle Enable when set to a one suppresses writes to the Rx FIFO when the FIFO becomes almost full as determined by the programmable almost full flag. FIFO writes will be re-enabled when the FIFO becomes almost empty. When this bit is a zero FIFO writes can occur whenever there is room left in the FIFO.

FIFO Loop Test B when set to a one allows both reading and writing of FIFO B from the PCI bus. This is used to test the FIFO.

Rx Invert, when set to a one, inverts the input data, when zero, the data is not inverted.

Rx Enable when set to a one enables the receiver state machine to receive messages. If Rx Enable is set to a zero the reception will stop after the current word is stored in the FIFO.

BIS2_UART

[$10] BiSerial II UART Control Register Port read/write

CONTROL UART	
DATA BIT	DESCRIPTION
31-13	Spare
12-4	Baud Rate = 3110400/n
3	Stop Two
2	Parity Odd
1	Parity Enable
0	UART Enable

FIGURE 9 PMC BISERIAL-II UART CONTROL REGISTER BIT MAP

Baud Rate determines the rate at which the transmit data is sent and the rate that the received data is expected to arrive. The 62.208 MHz oscillator is divided by this count to yield a 20x clock for the Rx sampling. The Tx clock is derived by pre-dividing the oscillator by 20 and then by this count. The receiver will re-sync whenever a transition is seen in the data if it is within one 20x clock of the expected bit boundary. This allows for substantial tolerance in the received baud rate. The data is sampled at the center of the bit period.

Stop Two when set to a one causes the transmitter to add two stop bits and the receiver to expect two stop bits. When this bit is a zero only one stop bit is used.

Parity Odd when set to a one causes the transmitter and receiver to use odd parity to calculate the parity bit, if enabled. When this bit is a zero, even parity is used.

Parity Enable when set to a one enables the calculation and reporting of parity bits and errors. When this bit is a zero, parity is not calculated, but a bit position is still added for the parity bit.

UART Enable when set to a one enables the UART transmitter and receiver to send and receive data respectively. When this bit is a zero the UART is disabled.

BIS2_STAT0

[$14] BiSerial II Status Port 0 read only

STATUS 0	
DATA BIT	DESCRIPTION
31-16	Spare
15	Interrupt Status
14	FIFO B Ready
13	Data B Ready
12	FIFO B Full
11	FIFO B Almost Full
10	FIFO B Half Full
9	FIFO B Almost Empty
8	FIFO B Empty
7	Spare
6	FIFO A Ready
5	Data A Ready
4	FIFO A Full
3	FIFO A Almost Full
2	FIFO A Half Full
1	FIFO A Almost Empty
0	FIFO A Empty

FIGURE 10 PMC BISERIAL-II STATUS REG 0 BIT MAP

When Interrupt Status is read as a one, it indicates that one or more latched interrupt conditions are true. In order for an actual system interrupt to occur, the interrupt enable for that condition and the Master Interrupt Enable must both be asserted. When this bit is zero, no interrupt conditions are pending.

When FIFO B Ready is read as a one, FIFO B is available to accept data. This means that it is not full and is not currently in the process of writing a word. When this bit is a zero data cannot be written.

When Data B Ready is read as a one, it indicates that a data word is available in the read holding register. This register will be filled whenever the FIFO is enabled and at least one word has been written to the FIFO. When this bit is a zero, no data is waiting to be read.

When FIFO B Full is read as a one, the FIFO is full; when it is a zero, the FIFO is not full.

When FIFO B Almost Full is read as a one, the FIFO is almost full as determined by the programmable offset flag registers. When this bit is zero the FIFO is below almost full.

When FIFO B Half Full is read as a one, the FIFO is half-full or more; when it is zero, the FIFO is below half-full.

When FIFO B Almost Empty is read as a one, the FIFO is almost empty as determined by the programmable offset flag registers. When this bit is zero the FIFO is above almost empty.

When FIFO B Empty is read as a one, the FIFO is empty although there could still be one more word in the read holding register (see Data B Ready). When this bit is zero there is data in the FIFO.

When FIFO A Ready is read as a one, FIFO A is available to accept data. This means that it is not full and is not currently in the process of writing a word. When this bit is a zero data cannot be written.

When Data A Ready is read as a one, it indicates that a data word is available in the read holding register. This register will be filled whenever the FIFO is enabled and at least one word has been written to the FIFO. When this bit is a zero, no data is waiting to be read.

When FIFO A Full is read as a one, the FIFO is full; when it is a zero, the FIFO is not full.

When FIFO A Almost Full is read as a one, the FIFO is almost full as determined by the programmable offset flag registers. When this bit is zero the FIFO is below almost full.

When FIFO A Half Full is read as a one, the FIFO is half-full or more; when it is zero, the FIFO is below half-full.

When FIFO A Almost Empty is read as a one, the FIFO is almost empty as determined by the programmable offset flag registers. When this bit is zero the FIFO is above almost empty.

When FIFO A Empty is read as a one, is read as a one, the FIFO is empty although there could still be one more word in the read holding register (see Data A Ready). When this bit is zero there is data in the FIFO.

BIS2_SW_IN

[$18] BiSerial II Switch Read Port read only

USER CONTROL SWITCH REGISTER	
DATA BIT	DESCRIPTION
11	Rev 3
10	Rev 2
9	Rev 1
8	Rev 0
7	UB7
6	UB6
5	UB5
4	UB4
3	UB3
2	UB2
1	UB1
0	UB0

FIGURE 11 PMC BISERIAL-II SWITCH READ BIT MAP

The Switch Read Port has the user bits. The user bits are connected to the eight dip-switch positions. The switches allow custom configurations to be defined by the user and for the software to identify a particular board by its switch settings and to configure it accordingly. The silk-screen is marked with the bit positions and '0' and '1' definitions.

The upper four bits are used to identify the revision of the Xilinx prom installed. This is useful for configuration control. The current revision is "0001".

BIS2_STAT1

[$1C] BiSerial II Status Port 1 read/write

STATUS 1	
DATA BIT	DESCRIPTION
31-14	Spare
13	Tx Done
12	Sync Lock Lost
11	Sync Lock Acquired
10	Clock Error Detected
9	Upper Sync Word Detected
8	Lower Sync Word Detected
7	UART Parity Error Detected
6	UART Framing Error Detected
5	UART Data Available
4	UART Tx Done
3	FIFO B Almost Full
2	FIFO B Almost Empty
1	FIFO A Almost Full
0	FIFO A Almost Empty

FIGURE 12 PMC BISERIAL-II STATUS REG 1 BIT MAP

All bits in this register are latched high when the appropriate condition occurs. They will remain high until they are explicitly cleared by writing to this address with a one in the corresponding bit position.

When Tx Done is read as a one, a message has been sent from the Tx FIFO and completed; when it is a zero, a message has not completed since this bit was cleared.

When Sync Lock Lost is read as a one, sync lock has been acquired and then lost. Sync lock occurs when three consecutive sync words are detected with the proper scan length separating them. Once sync lock is acquired three consecutive scans without a sync word being detected must occur before sync lock is lost. When this bit is zero sync lock has either not been acquired or is currently in effect.

When Sync Lock Acquired is read as a one, sync lock has occurred as described above; when it is zero, sync lock has not occurred since the bit was last cleared.

When Clock Error Detected is read as a one, the data strobes from the upper and lower data stream have been seen as not coherent at some point. When this bit is zero the data strobes have been coherent since the bit was last cleared.

When Upper Sync Word Detected is read as a one, a sync word has been seen on the upper data stream. When this bit is zero no sync word has been seen on the upper data stream since the bit was last cleared.

When Lower Sync Word Detected is read as a one, a sync word has been seen on the lower data stream. When this bit is zero no sync word has been seen on the lower data stream since the bit was last cleared.

When UART Parity Error Detected is read as a one, a parity error has been detected in a character received by the UART. When this bit is a zero no parity error has been detected since the bit was last cleared.

When UART Framing Error Detected is read as a one, a framing error has been detected in a character received by the UART. This means the input level was not high when a stop bit was expected. When this bit is a zero no framing error has been detected since the bit was last cleared.

When UART Data Available is read as a one, a character has been received by the UART. When this bit is a zero no character has been received since the bit was last cleared.

When UART Tx Done is read as a one, a character has been completely sent by the UART. When this bit is a zero no has been sent since the bit was last cleared.

When FIFO B Almost Full is read as a one, it indicates that the FIFO has become almost full, that is, it has gone from less than almost full to almost full or above. When this bit is a zero, the FIFO has not become almost full.

When FIFO B Almost Empty is read as a one, it indicates that the FIFO has become almost empty, that is, it has gone from above almost empty to almost empty or below. When this bit is a zero, the FIFO has not become almost empty.

When FIFO A Almost Full is read as a one, it indicates that the FIFO has become almost full, that is, it has gone from less than almost full to almost full or above. When this bit is a zero, the FIFO has not become almost full.

When FIFO A Almost Empty is read as a one, it indicates that the FIFO has become almost empty, that is, it has gone from above almost empty to almost empty or below. When this bit is a zero, the FIFO has not become almost empty.

BIS2_FIFOTX

[$20] BiSerial II Tx FIFO write-read port
The BiSerial II supports 32-bit writes to the transmit data FIFO. Data is aligned D31-0. Normally this port is only written to, but for loop-back testing the contents of the FIFO can be read out over the PCI bus. The FIFO loop test A bit in the Tx control register must be set to a one in order to accomplish this. The engineering kit contains software, which performs a Tx FIFO loop-back test. Once data is read from the FIFO it is no longer available for transmission.

BIS2_FIFORX

[$24] BiSerial II Rx FIFO write-read port

The BiSerial II supports 32-bit reads from the receive data FIFO. Data is aligned D31-0. Normally this port is only read from, but for loop-back testing the contents of the FIFO can be written from the PCI bus. The FIFO loop test B bit in the Rx control register must be set to a one in order to accomplish this. The engineering kit contains software, which performs an Rx FIFO loop-back test. Once data is read from the FIFO it is no longer available.

BIS2_DIR_TERM

[$28] BiSerial II Direction and Termination Register Port read/write

CONTROL DIR_TERM REGISTER		
DATA BIT	DESCRIPTION	
13-0	DIRection 13-0	0 = read 1 = drive
29-16	TERMination 13-0	1 = terminated

FIGURE 13 PMC BISERIAL-II DIRECTION TERMINATION CONTROL BIT MAP

The direction for each of the 32 differential pairs is controlled through this port. The port defaults to zero, which corresponds to tri-stating the drivers and no terminations enabled.

Pull-up and Pull-down resistors built into some '485 interface devices may make the signal appear to be driven (if open) when in the tri-stated mode. Enabling the termination on a tri-stated line will yield approximately 2.5V on each side of the tri-stated driver.

The base design of the PMC_BiSerial II_NVY1 sets direction bits 4 - 7 high (outputs), and direction bits 9, 10 low (inputs). Currently the forced bits are read-write but have no effect.

CONTROL	CORRESPONDING IO BIT(S)
DIR_0..7	IO_0..7
DIR8	IO_8..11
DIR9	IO_12..15
DIR10	IO_16..19
DIR11	IO_20..23
DIR12	IO_24..27
DIR13	IO_28..31

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others it will make sense to use the onboard terminations.

The terminations for the receive groups should be set to terminate with the user software in most cases. [term_9 and term_10]

CONTROL	CORRESPONDING IO BIT(S)
TERM_0..7	IO_0..7
TERM_8	IO_8..11
TERM_9	IO_12..15
TERM_10	IO_16..19
TERM_11	IO_20..23

TERM_12	IO_24..27
TERM_13	IO_28..31

BIS2_SYNCW1H

[$2C] BiSerial II Sync Word 1H Register Port read/write

RX SYNC 1H	
DATA BIT	DESCRIPTION
31-24	Spare
23-0	Upper 24 Bits of Sync Word 1 (Ping Sync)

FIGURE 14 PMC BISERIAL-II RX SYNC WORD 1H REGISTER BIT MAP

The Sync word registers allow the user to specify the sync patterns that the circuit looks for to establish data framing and control data storage. This register contains the upper 24 bits of the 48-bit ping sync word.

BIS2_SYNCW1L

[$30] BiSerial II Sync Word 1L Register Port read/write

RX SYNC 1L	
DATA BIT	DESCRIPTION
31-24	Spare
23-0	Lower 24 Bits of Sync Word 1 (Ping Sync)

FIGURE 15 PMC BISERIAL-II RX SYNC WORD 1L REGISTER BIT MAP

The Sync word registers allow the user to specify the sync patterns that the circuit looks for to establish data framing and control data storage. This register contains the lower 24 bits of the 48-bit ping sync word.

BIS2_SYNCW2H

[$34] BiSerial II Sync Word 2H Register Port read/write

RX SYNC 2H	
DATA BIT	DESCRIPTION
31-24	Spare
23-0	Upper 24 Bits of Sync Word 2 (Scan Sync)

FIGURE 16 PMC BISERIAL-II RX SYNC WORD 2H REGISTER BIT MAP

The Sync word registers allow the user to specify the sync patterns that the circuit looks for to establish data framing and control data storage. This register contains the upper 24 bits of the 48-bit scan sync word.

BIS2_SYNCW2L

[$38] BiSerial II Sync Word 2L Register Port read/write

RX SYNC 2L	
DATA BIT	DESCRIPTION
31-24	spare
23-0	Lower 24 Bits of Sync Word 2 (Scan Sync)

FIGURE 17 PMC BISERIAL-II RX SYNC WORD 1L REGISTER BIT MAP

The Sync word registers allow the user to specify the sync patterns that the circuit looks for to establish data framing and control data storage. This register contains the lower 24 bits of the 48-bit scan sync word.

BIS2 _UART_DATA

[$3C] BiSerial II UART Data Port read/write

UART DATA	
DATA BIT	DESCRIPTION
31-8	spare
7-0	UART Data

FIGURE 18 PMC BISERIAL-II UART DATA REGISTER BIT MAP

Writing a character to this address causes it to be loaded into the UART shift register with start, stop and parity bits added and shifted out over the selected IO line. When the last bit is sent, the UART Tx done status bit is set.

When a character is received, the UART data available status bit is set and the contents of the Rx holding register can be read from this address.

Flag Insertion

Whenever a sync sequence is recognized a four-bit pattern will be inserted. This pattern replaces the most significant four bits in the third 16-bit word following the sync word. When a ping sync (sync word 1) is detected a "0110" pattern will be inserted, when a scan sync (sync word 2) is detected a "1001" pattern will be inserted.

Interrupts

PMC BiSerial-II interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with a PMC BiSerial-II interrupt the software must read the status register to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

For example, the PMC BiSerial-II Tx state machine generates an interrupt request when a transmission is complete and the Tx done int enable and Master interrupt enable bits in the BIS2_INTEN register are set. The transmission is considered complete when the last bit is output from the output shift register.

The interrupt is mapped to INTA on the PMC connector, which is mapped to a system interrupt when the PCI bus configures. The source of the interrupt is obtained by reading BIS2_STAT1. The status remains valid until that bit in the status register is explicitly cleared.

When an interrupt occurs, the Master interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the latched bit and set the Master interrupt enable bit high again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the BIS2_STAT1 register. Alternatively, the conditions of interest can be enabled, but the Master interrupt enable left disabled. Then the interrupt status bit in BIS2_STAT0 can be monitored. If one of the enabled conditions occurs, the interrupt status bit will be set, but unless the Master interrupt enable is set, a system interrupt will not occur.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable with the following pins connected. Select either Input1 or Input0, but not both at the same time, as this will double terminate the data lines and degrade the signal amplitude. The UART signals have only one input per output and are therefore not restricted in this way.

SIGNAL	OUTPUT	INPUT0	INPUT1

Data0+	7	21	24
Data0-	41	55	58
Data1+	9	22	26
Data1-	43	56	60
UART0+	12	32	
UART0-	46	66	
UART1+	11		28
UART1-	45		62

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC BiSerial-II-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V[unused]	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 19 PMC BISERIAL-II PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC BiSerial-II-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V[unused]		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 20 PMC BISERIAL-II PN2 INTERFACE

BiSerial II Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC BiSerial-II. Also, see the User Manual for your carrier board for more information. GND* is a plane which is tied to GND through a 1206 0Ω resistor. DC, AC or open are options. For customized version, or other options, contact Dynamic Engineering.

IO_0p	IO_0m	1	35
IO_1p	IO_1m	2	36
IO_20p	IO_20m	3	37
IO_2p	IO_2m	4	38
IO_21p	IO_21m	5	39
IO_3p	IO_3m	6	40
IO_4p [TXO_DATA+]	IO_4m [TXO_DATA-]	7	41
IO_22p	IO_22m	8	42
IO_5p [TX1_DATA+]	IO_5m [TX1_DATA-]	9	43
IO_23p	IO_23m	10	44
IO_6p [UART1_TX+]	IO_6m [UART1_TX-]	11	45
IO_7p [UARTO_TX+]	IO_7m [UARTO_TX-]	12	46
IO_24p	IO_24m	13	47
IO_8p	IO_8m	14	48
IO_25p	IO_25m	15	49
IO_9p	IO_9m	16	50
IO_10p	IO_10m	17	51
IO_26p	IO_26m	18	52
IO_11p	IO_11m	19	53
IO_27p	IO_27m	20	54
IO_12p [RXOL_ DATA+]	IO_12m [RXOL_ DATA-]	21	55
IO_13p [RXOU_DATA+]	IO_13m [RXOU_DATA-]	22	56
IO_28p	IO_28m	23	57
IO_14p [RX1L_ DATA+]	IO_14m [RX1L_ DATA-]	24	58
IO_29p	IO_29m	25	59
IO_15p [RX1U_ DATA+]	IO_15m [RX1U_ DATA-]	26	60
IO_30p	IO_30m	27	61
IO_16p [UART1_RX+]	IO_16m [UART1_RX-]	28	62
IO_31p	IO_31m	29	63
IO_17p	IO_17m	30	64
GND*	GND*	31	65
IO_18p [UARTO_RX+]	IO_18m [UARTO_RX-]	32	66
GND*	GND*	33	67
IO_19p	IO_19m	34	68

FIGURE 21 PMC BISERIAL-II FRONT PANEL INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC BiSerial-II Module routed to Pn4. Also, see the User Manual for your carrier board for more information.

IO_0p		IO_0m		1	2
IO_1p		IO_1m		3	4
IO_2p		IO_2m		5	6
IO_3p		IO_3m		7	8
IO_4p	TXO_DATA+	IO_4m	TXO_DATA-	9	10
IO_5p	TX1_DATA+	IO_5m	TX1_DATA-	11	12
IO_6p	UART1_TX+	IO_6m	UART1_TX-	13	14
IO_7p	UARTO_TX+	IO_7m	UARTO_TX-	15	16
IO_8p		IO_8m		17	18
IO_9p		IO_9m		19	20
IO_10p		IO_10m		21	22
IO_11p		IO_11m		23	24
IO_12p	RXOL_DATA+	IO_12m	RXOL_DATA-	25	26
IO_13p	RXOU_DATA+	IO_13m	RXOU_DATA-	27	28
IO_14p	RX1L_DATA+	IO_14m	RX1L_DATA-	29	30
IO_15p	RX1U_DATA+	IO_15m	RX1U_DATA-	31	32
IO_16p	UART1_RX+	IO_16m	UART1_RX-	33	34
IO_17p	UARTO_RX+	IO_17m	UARTO_RX-	35	36
IO_18p		IO_18m		37	38
IO_19p		IO_19m		39	40
IO_20p		IO_20m		41	42
IO_21p		IO_21m		43	44
IO_22p		IO_22m		45	46
IO_23p		IO_23m		47	48
IO_24p		IO_24m		49	50
IO_25p		IO_25m		51	52
IO_26p		IO_26m		53	54
IO_27p		IO_27m		55	56
IO_28p		IO_28m		57	58
IO_29p		IO_29m		59	60
IO_30p		IO_30m		61	62
IO_31p		IO_31m		63	64

FIGURE 22 PMC BISERIAL-II PN4 INTERFACE

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC BiSerial-II when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The PMC BiSerial-II does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the BiSerial II pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68-screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68
[http://www.dyneng.com/HDEterm68.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC BiSerial-II is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BiSerial II design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
support@dyneng.com

Specifications

Host Interface:	PCI Mezzanine Card - 32 bit
Serial Interface:	RS-485 TXO_Data, TX1_Data, RXOL_Data, RXOU_Data, RX1L_Data, RX1U_Data, UART0_Tx, UART1_Tx, UART0_Rx, UART1_Rx
Tx Data rates generated:	15.552, 10.368, 7.776, 6.2208, 5.184, 4.4434, 3.888 MHz with 62.208 MHz oscillator. Other rates are available with different oscillator installation.
Rx Data rates accepted:	Continuous from 5.2 to 12.4 Mbps with 62.208 MHz oscillator.
UART Data rates:	3110400/n, n = 1..511 with 62.208 MHz oscillator.
Software Interface:	Control Registers, Status Ports, FIFOs
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses
Interrupt:	Tx interrupt at end of transmission Rx Clock Error Rx Sync Lock Acquired Rx Sync Lock Lost Upper sync detected Lower sync detected Tx Programmable Almost Empty Tx Programmable Almost Full Rx Programmable Almost Empty Rx Programmable Almost Full UART parity error UART framing error UART Rx data available UART Tx done
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC BiSerial-II NVY1	PMC Module with 2 TX, 2 paired Rx serial, 2 UART Tx and 2 UART Rx channels Programmable TX and UART data rates Manchester encoded data inputs and outputs RS-485 drivers and receivers 32 bit data interface
Eng Kit–PMC BiSerial-II	HDEterm68 - 68 position screw terminal adapter http://www.dyneng.com/HDEterm68.html HDEcabl68 - 68 IO twisted pair cable http://www.dyneng.com/HDEcabl68.html Technical Documentation, 1. PMC BiSerial-II Schematic 2. PMC BiSerial-II NVY1 Reference test software Data sheet reprints are available from the manufacturer's web site reference software: C souirce code requires WinRT.

***Note**: The Engineering Kit is strongly recommended for first time* PMC BiSerial-II *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.