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SpaceWireBK Win10ReadMe

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Connection of incompatible hardware is likely to cause serious damage.

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Introduction

The SpWrBkUserApp test application contains three menus accessed by single character commands entered in the test window created by double-clicking on the SpWrBkUserApp.exe icon. These commands are 'A', 'I' or 'X'. When the window is first opened, the ATP (Acceptance Test Procedure) menu will be displayed. Entering an 'I' will bring up the Divided Clock test menu. Entering an 'X' will bring up the File Xfer test menu. Entering an 'A' will return to the ATP test menu.

Main (ATP) Menu

The tests in this menu are listed roughly in order of increasing complexity.

Test 0: (Null test) This test does nothing but call an empty test and increment the pass count.

Test 1: (Read switch) This test reads the 8-position user switch and report this value whenever it is changed. The test expects a value of 0x00 when the test begins. If the switch is set to all zeros, the pass count will increment continuously until the value is changed or the test is stopped. If the switch is not set to all zeros, the value will be printed and the failure count will increment to 1, after which the pass count will continuously increment. Each time the switch value is changed, the new value will be displayed and the fail count will be incremented by 1, after which the pass count will continuously increment. Exercising each of the eight bits verifies their connection and functionallity. The switch is intended to be used by the user for any purpose desired. To distinguish between multiple installed boards, to indicate different firmware or software configurations, etc.

Test 2, 3 and 4: These tests are register write/read tests to verify the internal address and data buses.

Test 5: (Force Interrupt tst) This test exercises the channel interrupts using the force interrupt channel configuration register bit, with kernel event objects to signal occurrence of an interrupt.

Test 6: (FifoTstAll) This test uses DMA to fill the channel FIFOs with a data pattern and then read and verify the data as well as the FIFO status flags. It tests channels 0-3 sequentially.

Test 7: (PLL program test) The first time this test is run it will ask for a PLL configuration file (*.jed). If the current contents of the PLL internal registers do not match this file, the PLL will be programmed from the file contents. Subsequent loops of the test continuously read and verify the PLL internal register data. This test requires connection from a suitable JTAG programming port to the JTAG header (J1).

Test 8: (Reprogram PLL) Resets the flag that indicates that the PLL has been programmed and then asks for a PLL configuration file and, if the file does not match the PLL internal register data, reprograms the PLL from the file contents. The test only runs a single loop; it is used to program new PLL frequencies. This test requires connection from a suitable JTAG programming port to the JTAG header (J1).

Tests 9-24: These tests fill each channel's TX FIFO with a data pattern and then transfers that data over the SpaceWire link to the same channel's RX FIFO and then reads and verify the data as well as the FIFO status flags. All combinations of single word access and DMA are used. These tests require the respective SpaceWire single-channel loop-back connection.

Tests 9-12: Uses single-word writes and single-word reads.

Tests 13-16: Uses DMA writes and single-word reads.

Tests 17-20: Uses single-word writes and DMA reads.

Tests 21-24: Uses DMA writes and DMA reads.

Tests 25-34: These tests transfer 16 Mbytes of data between every possible combination of channels including transfers to themselves using 1 Mbyte - n packet-lengths of consecutive values of n(mod 4). These tests require the appropriate SpaceWire channel-to-channel or single-channel loop-back connection.

Tests 35-44 These tests transfer 16 Mbytes of data between every possible combination of channels including transfers to themselves using a single packet-length value continually reused. These tests require the appropriate SpaceWire channel-to-channel or single-channel loop-back connection.

Tests 45-54: These tests send timecode tokens between every possible combination of channels across a single SpaceWire link. These tests require the appropriate SpaceWire channel-to-channel or single-channel loop-back connection.

Test 55: (Tmcd ch 0-2^1-3 PCI) This test sends timecode tokens through all four channels using an external SpaceWire link between channel 0 and channel 2, an internal link between channel 2 and channel 1 and an external SpaceWire link between channel 1 and channel 3. This test requires SpaceWire channel-to-channel connections between channels 0<=>2, and channels 1<=>3.

Test 56: (Tmcd ch 1-1^0-2^3-3) This test sends timecode tokens through all four channels using an external SpaceWire link between channel 1 and itself, an internal link between channel 1 and channel 0, an external SpaceWire link between channel 0 and channel 2, an internal link between channel 2 and channel 3 and an external SpaceWire link between channel 3 and itself. This test requires a SpaceWire channel-to-channel connections between channels 0<=>2, and SpaceWire single-channel loop-back connections on channel 1 and channel 3.

Test 57: (SpaceWire ATP test1) This test performs the series of internal tests individually called out by tests 2, 3, 4, 5 and 6. No external connections are required to perform this test.

Test 58: (PCI ATP Multi-Freq) This test performs the Acceptance Test Procedure function for the PCI-SpaceWire. SpaceWire channel-to-channel connections between channels 0<=>2, and channels 1<=>3 are required.

Test 59: (PCIe ATP Multi-Freq) This test performs the Acceptance Test Procedure function for the PCIe-SpaceWire. SpaceWire channel-to-channel connections between channels 0<=>2, and channels 1<=>3 are required.

Test 60: (PC104p ATP Multi-Freq) This test performs the Acceptance Test Procedure function for the PC104p-SpaceWire. SpaceWire channel-to-channel connections between channels 0<=>2, and channels 1<=>3 are required.

Test 61: (PMC ATP Multi-Freq) This test performs the Acceptance Test Procedure function for the PMC-SpaceWire. SpaceWire channel-to-channel connections between channels 0<=>2, and SpaceWire single-channel loop-back connections on channel 1 and channel 3 are required.

Divided Clock Menu

Using a divided clock allows for I/O rates below 10 Mbits/second. 10 MHz is the minimum programmed clock rate that meets the SpaceWire specification requirements for establishing a SpaceWire connection.

Test 0: (Null test) This test does nothing but call an empty test and increment the pass count.

Tests 1-4: These tests check the performance of individual channel's FIFOs using DMA.

Test 5: (Reprogram PLL) Resets the flag that indicates that the PLL has been programmed and then asks for a PLL configuration file and, if the file does not match the PLL internal register data, reprograms the PLL from the file contents. The test only runs a single loop; it is used to program new PLL frequencies. This test requires connection from a suitable JTAG programming port to the JTAG header (J1).

Tests 6-15: These tests transfer 1 Mbyte of data between every possible combination of channels including transfers to themselves using an I/O bit rate equal to the programmed clock divided by 2 and using 1 Mbyte - n packet-lengths of consecutive values of n(mod 4). These tests require the appropriate SpaceWire channel-to-channel or single-channel loop-back connection.

Tests 16-25: These tests transfer 1 Mbyte of data between every possible combination of channels including transfers to themselves using an I/O bit rate equal to the programmed clock divided by 3 and using 1 Mbyte - n packet-lengths of consecutive values of n(mod 4). These tests require the appropriate SpaceWire channel-to-channel or single-channel loop-back connection.
Tests 26-35: These tests transfer 1 Mbyte of data between every possible combination of channels including transfers to themselves using an I/O bit rate equal to the programmed clock divided by 4 and using 1 Mbyte - n packet-lengths of consecutive values of n(mod 4). These tests require the appropriate SpaceWire channel-to-channel or single-channel loop-back connection.

Tests 36-45: These tests transfer 1 Mbyte of data between every possible combination of channels including transfers to themselves using an I/O bit rate equal to the programmed clock divided by 5 and using 1 Mbyte - n packet-lengths of consecutive values of n(mod 4). These tests require the appropriate SpaceWire channel-to-channel or single-channel loop-back connection.

File Transfer Menu

Test 0: (Null test) This test does nothing but call an empty test and increment the pass count.

Tests 1-4: These tests open and read the specified file and send the contents from the selected SpaceWire channel. In order to successfully transfer a file, a file reception must have been previously setup on a different channel either on the same board or another in the same chassis or another chassis. If the specified file is not in the same folder as the test executable, the file name must be prepended with the absolute or relative path. The length of the file is obtained and entered as the packet-length for the transfer. The contents of the file is written to the transmit FIFO and the data is sent over the SpaceWire link.

Tests 5-8: These tests setup file receptions on the selected SpaceWire channels. When selected, the user will be prompted for a name to assign to the received file and the file is opened for writing. The selected channel then waits for a packet received interrupt, reads the length of the received packet and uses DMA to read the file data and write it to the specified file.