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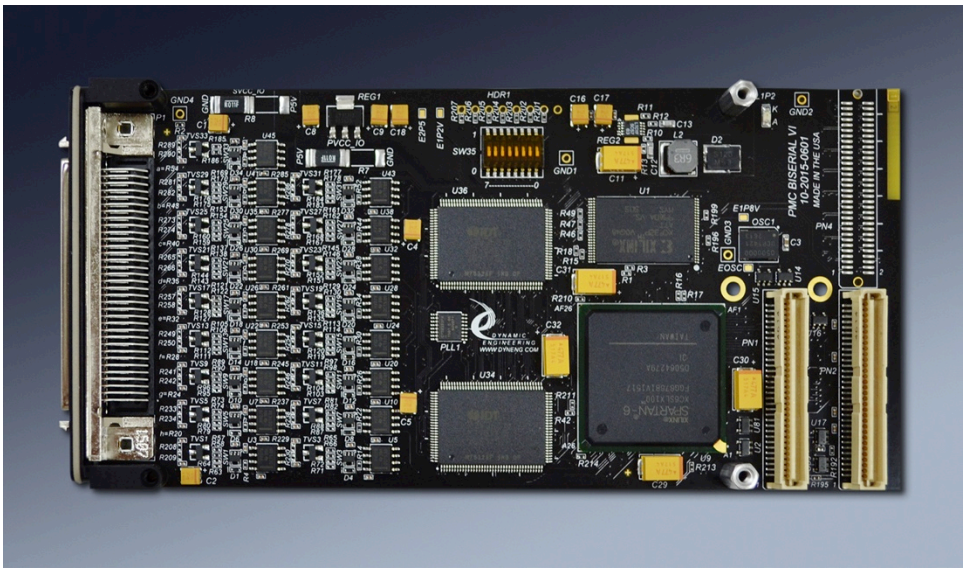
User Manual

PMC-BiSerial-VI-S311

Hardware Manual

Two Port Bi-directional Serial Data Interface PMC Module



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PMC-BiSerial-VI-S311
Bi-directional Serial Data Interface
PMC Module

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

PMC-BISERIAL-VI is part of the Dynamic Engineering family of modular I/O. PMC-BISERIAL-VI-S311 is a PMC with options for bezel and rear IO, multiple modes of operation, 8K bytes of storage per Tx or Rx node. 2 Full Duplex Ports.

PMC-BISERIAL-VI-S311 uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with PMC-BISERIAL-VI-S311, please let us know. We may be able to do a special build with a different height connector to compensate.

The PMC-BISERIAL conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

Feature Table:
1. 4Kx32 FIFO's for Rx and Tx data storage per channel
3. Multiple clock sources – 10 MHz, PCI/2, External
4. Clock Generator per port with programmable divider and clock selection
5. 8 position Switch
6. Windows driver and reference software. Linux and VxWorks by request.
7. Industrial temperature components [-40 ⇔ +85C]
8. Programmable interrupts

Custom interfaces are available. We will redesign the state machines and create a custom interface protocol. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

Differential I/O is available on the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). [LVDS is an option]. The RS-485 input signals are selectively terminated with 100Ω. The resistors are in discrete packages to allow individual termination options for custom formats and protocols. There are 32/34 transceivers for the IO. The transceivers, and terminations are individually programmable to allow for any configuration.

The configuration implemented in the S311 uses four outputs for Tx data, Tx burst-clock Tx request, and Rx ready; and four inputs for Rx data, Rx burst-clock, Rx request, and Tx ready per port. In addition the External Reference Clock is assigned to an IO. The terminations on the IO are programmable.

All configuration registers support read and write operations for maximum software convenience. All addresses are long word aligned.

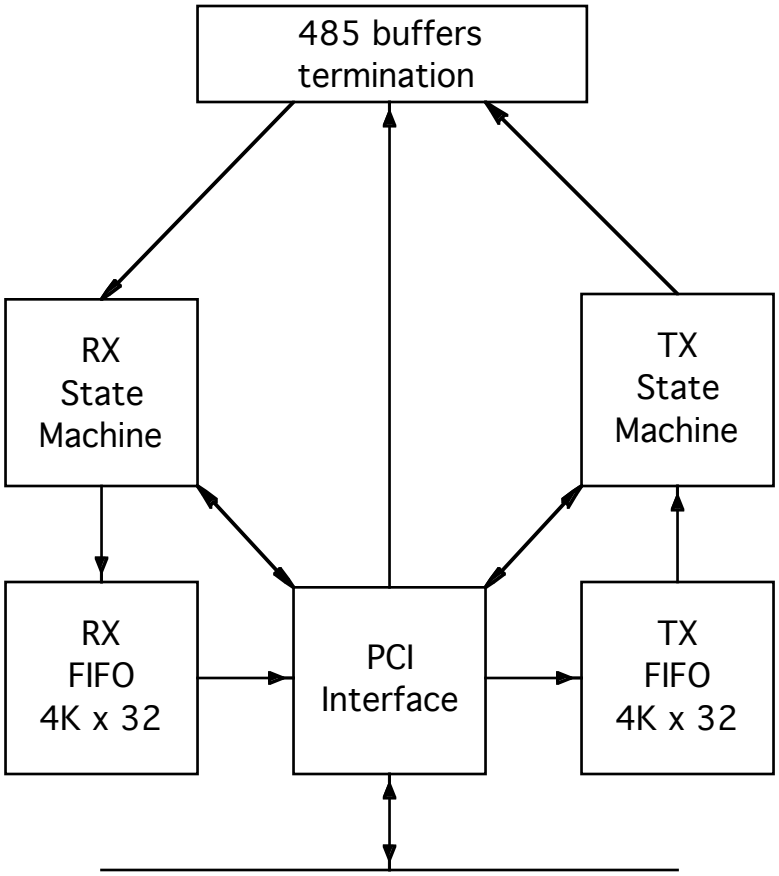

FIGURE 1 PMC-BISERIAL-VI-S311 BLOCK DIAGRAM

The PMC-BiSerial-VI-S311 implements the Northrop Grumman S-311 interface protocol. Diagram is shown for 1 port. 2 ports are implemented. This protocol uses a burst clock to shift 18 bits of data. The data changes on the rising edge of the clock and is valid on the falling edge. The first bit is the sync bit, which is always high and the next 8 bits are the upper byte of the data shifted out MSB first. The next bit is the mode bit, which is zero for a data word and one for a command word. The final 8 bits are the lower byte of data shifted out MSB first.

Two additional signals are used in this protocol, request and ready. The request signal is asserted high by the transmitter at least two clock periods before the first clock. The request signal also remains asserted at least two clock periods after the falling edge of the last clock. After request goes low, at least four clock periods must elapse before it is reasserted.

The ready signal is asserted high by the receiver when it is ready to receive data i.e. it has been started and the Rx FIFO is not full. The ready signal can remain high between words as long as the receiver is able to receive data. No data will be transmitted unless ready is high or programmed to be ignored.

The serial channels are each supported by a 4K by 32 bit FIFO (see figure 1). The FIFO supports long word reads and writes. A path exists for loop-back testing of each FIFO. The PCI and PMC data paths are 32 bits wide.

As the serial receive channel receives data, MSB first, it is stored in 18-bit words with the sync bit in the MSB (bit 17), the mode bit repositioned to bit 16 and the 16 data bits stored in bit 15 down to 0. The host can poll the empty flag status or use the programmable FIFO Almost Full flag to determine when data is available. The message can be read directly from the input FIFO.

The Output channel has a separate 4K x 32 FIFO. The FIFO is written as long words with the sync bit in bit position 17, the mode bit in bit position 16 and the 16 data bits in bit positions 15 to 0. Data is sent MSB first with the sync bit first followed by eight data bits, the mode bit, and the final eight data bits. Data is sent whenever the transmitter is enabled and data is stored within the FIFO and the ready signal is asserted from the receiver. Transmission completes and the transmitter is disabled when the FIFO becomes empty.

Interrupts are supported by PMC-BiSerial-VI. For the S311 version, interrupts can be generated by the following conditions: transmission complete; transmitter almost empty; receiver almost full; receiver overflow; and a receiver interrupt, which can be configured to respond to any word received, or for a word received with a specific mode bit value, either zero or one.

The interrupts are individually maskable. A master interrupt enable is provided at the base and port level. Force Interrupt is a SW generated interrupt to support testing purposes. The interrupt occurs on INTA. The FIFO levels and other status are also available for operating in a polled mode, if desired. The base level status register reports the PORT interrupt activity to allow single read determination of interrupt origin when interrupts are shared.

Theory of Operation

PMC-BISERIAL-VI is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design. In standard configuration, the PMC-BiSerial-VI is a Type II mechanical with legal height components on the rear of the board and one slot wide, with 10 mm inter-board height.

PMC-BISERIAL-VI-S311 is designed for transferring data from one point to another with a specific serial protocol. It features a Xilinx FPGA, which contains all of the registers and protocol controlling elements of the BiSerial design.

A logic block within the Xilinx controls the PCI interface to the host CPU. This design uses the Dynamic Engineering PCI core.

PMC-BISERIAL-VI-S311 is designed to transmit and receive data using the Northrop Grumman S-311 protocol. This protocol uses and 18 bit word to transfer 16 data bits and a mode bit indicating whether the word is data or command. In addition, a sync bit, which is always high is sent as the first bit of a serial transfer. The data is written and read over the PCI bus with the sync bit as bit 17 of a 32-bit word, the mode bit as bit 16 and the 16 data bits occupying bit positions 15 through 0. However, when the bits are sent serially the sync bit is sent first followed by data bit 15 down to 8, next the mode bit is sent followed by data bits 7 down to 0. The S311 clock speed can be anything from 0 to 1 MHz, and is nominally 250 kHz.

The receiver uses the PCI clock to sample the received S311 clock to detect transitions and capture the data. With a 10:1 ratio the upper limit of the received data is about 3.1MHz.

Clock reference sources include an on-board 32 MHz oscillator [converted to 10 MHz with DCM], the PCI clock divided by 2, and an External Reference clock. The Transmit reference clock is available at the base rate or after a programmable 12-bit divider. PMC-BiSerial-VI has features to allow muxed clocks to be sent off chip and routed back on as clock lines for cases where the clock reference is asynchronous to the source. This feature is used to allow the multiple sources for the divider without taking the clocks off long lines. Please refer to the memory map for more details.

An interrupt can be generated by five conditions: transmit complete, determined by the transmit FIFO going empty; the transmit FIFO programmable almost empty; the receive FIFO almost full; receiver overflow, which occurs when an

attempt is made to write to a full FIFO; and an additional receive interrupt, which can be configured to respond to any word received, or only words with mode bit zero, or only words with mode bit one. These conditions are latched until cleared by writing a one to the corresponding bit of the interrupt status register. Each interrupt is individually maskable by bits in the transmit and receive control registers and there is a master interrupt enable.

The receiver can also be configured to selectively store only words with mode bit equal to one or only words with mode bit equal to zero.

The values used for the almost empty and almost full FIFO flags are programmable and stored into a configuration register within each port. The Almost full function uses Greater Than to trigger and the Almost Empty uses Less Than to trigger. It is recommended to allow enough room to have SW respond before overflowing or under-running.

The time represented by the programmed FIFO space to interrupt is based on the serial frequency and number of bits. With 250 KHz. Each bit represents 4 uS. With 18 bits per word, a word represents 72 uS. A fairly small count can be used as 15 words is more than 1 mS. Remember to scale for faster serial rates.

Address Map

Base Address Map

Function		Offset	function	Type
Port0Clk	EQU	x00	0 Port 0 Clk Sel	read/write
Port1Clk	EQU	x04	1 Port 1 Clk Sel	read/write
Switch	EQU	x08	2 Switch & Revision	read only
Status	EQU	x0C	3 Base status register	read only
Port0	EQU	x40	Base Address for Port 0	R/W w/ 16 LW
Port1	EQU	x80	Base Address for Port 1	R/W w/ 16 LW

FIGURE 2 PMC-BISERIAL-VI-S311 BASE INTERNAL ADDRESS MAP

The address map provided is for the Base Functions within PMC-BiSerial-VI-S311. The addresses are all offsets from a base address. The carrier board the PMC is installed into provides the base address.

VendorId = 0xDCBA. CardId = 0x0068. Current Major revision = 0x03

Port Address Map

Function		Offset	function	Type
ChanCntl	EQU	x00	0 Port control register	read/write
ChanStatus	EQU	x04	1 Port Status	read/write
ChanWordCnt	EQU	x08	2 Port Received Word Count	read/write
ChanTxFIFO	EQU	x0C	3 Tx FIFO Access	read/write
ChanRxFIFO	EQU	x10	4 Rx FIFO Access	read/write
ChanFifoLvl	EQU	x14	5 AFL & AMT Count	read/write
PreReadTxFifo	EQU	x18	6 Write to read from Tx FIFO	write only
ChanTerm	EQU	x1C	7 Termination Control	read/write
ChanFifoCnt	EQU	x20	8 FIFO Counts	read

FIGURE 3 PMC-BISERIAL-VI-S311 PORT INTERNAL ADDRESS MAP

The address map provided is for the Port Functions within PMC-BiSerial-VI-S311. The addresses are all offsets from a port address.

Programming

Programming the PMC-BISERIAL-VI requires only the ability to read and write data from the host. The PMC Carrier board determines the base address. This documentation refers to the first user address for the position the PMC is installed in as the base address.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial-VI-S311 driver to communicate. For example in Win 7 there is a semi-automatic installation procedure built in to load the .sys and .inf files to update the system allowing user level access to the HW.

In order to receive data the software is only required to enable the Rx state machine. If desired, data filtering can be configured and interrupts can be enabled. Data will be loaded into the FIFO as it is received.

If interrupts are used, the interrupt service routine should be loaded and the mask bits should be set. After the interrupt is received, appropriate action can be taken. The Base Status register has indication of the port or ports with active Interrupts. The active port status can be read to determine the cause. The port status is “sticky” – writing back to status register with the same bit set will clear that bit.

The end of transmission interrupt indicates the Tx message has been completed.

Before transmitting data, the FIFO is loaded. If the clock rate desired is something other than the default rate then the rate should be selected. Be sure to set the clock source and rate bits appropriately. Once the complete message is loaded and the controls set, the start bit can be set to cause the transfer to begin. If a slow clock rate is selected and a long message is sent, data can be loaded during transmission to save operational time. Care must be taken to insure that the FIFO does not become empty prematurely, or the transmission will terminate. When the Tx interrupt is received the transmission has been completed and another message can be loaded. All that needs to happen for a second message to be sent is to load the FIFO and set the start bit.

To operate in a polled mode, read the Status register during the transfer and take appropriate action when the full, empty or programmable flag shows that there is data to read or space to write. The PAE flag is implemented to provide an almost empty interrupt to allow the TX side to operate in an interrupt driven mode with longer messages. Similarly the PAF can be used to provide an almost full interrupt for the receive side to allow interrupt driven long message capability.

Base Register Definitions

PortnClk

x00, x04 Clock Control Register Port read/write

Port Clock Control

DATA BIT	DESCRIPTION
31-18	spare
17	ForceInt [Port0 only]
16	MasterIntEn [Port 0 only]
15	spare
14-13	clock pre-selector
12	clock post-selector
11-0	clock divisor

FIGURE 4 PMC-BISERIAL-VI-S311 BASE CONTROL REG

Port 0 and Port 1 Clk register Definitions. Port 0 has the additional bits for Master Interrupt Enable and Force Interrupt. All bits are active high, and are reset on power-up.

ForceInt is used for test and software development purposes to create an interrupt request: 1 = assert interrupt request. 0 = normal operation. This is useful to stimulate interrupt acknowledge routines for development. Requires MasterIntEn to be set.

MasterIntEn when '1' gates all interrupts through to the PCI host. When '0' the interrupts can be used for status without interrupting the host.

Clock Pre-Selector

00	10 MHz
01	10 MHz
10	external
11	PCI clock/2

The clock pre-selector is used to select which reference clock to use with the divisor hardware (the clock source). The external clock is received on IO(0) for Port0 and IO(1) for Port1. The PCI clock rate is prescaled with divide by 2 as shown.

Divisor [11-0] is the clock divisor select bits. A counter divides the clock source. The reference clock for the counter is selected with the CLK Pre-Selector. The output frequency is [reference / [2(n+1)], n $\geq$ 1. The reference oscillator is 10 MHz in frequency. The counter divides by n+1 due to counting from 0 to n before

rolling over. The output is then divided by two to produce a square wave output.

Post Selector when '1' sets clock out to clock divided, when '0', clock out is set to the reference clock specified by the pre-selector.

Switch

X08 Switch & Revision Read Port read only

Switch & Revision PORT

DATA BIT	DESCRIPTION
31-24	spare
23-16	Minor Revision
15-8	Major Revision
7-0	Switch Input

FIGURE 5 PMC-BISERIAL-VI-S311 SWITCH & STATUS REG

The Switch Read Port returns the setting on the dipswitch. The switches allow custom configurations to be defined by the user and to identify individual units in a system with multiple S311's. The silk-screen is marked with the '0' and '1' definitions.

The Major Revision is rolled when major updates are made. The current revision is 3 indicating the port to the PMC-BiSerial-VI platform and addition of a second port plus additional features.

The Minor Revision is updated within a major revision to indicate more subtle improvements.

SW can use the Revision to "know" what features are available with the installed HW and to alert the user if a particular board needs to have the FLASH updated.

Major Revisions :
1 original Release 2002
2 update to delivery configuration
3 Port to PMC-BiSerial-VI, add second port 6/2018

Status

x0C Base Status Register Port read only

CONTROL TX	
DATA BIT	**DESCRIPTION**
31	IntRqst
30-4	spare
1	IntPort1
0	IntPort0

FIGURE 6 PMC-BISERIAL-VI-S311 TX CONTROL REGISTER BIT MAP

IntRqst when ‘1’ tells indicates an interrupt request is potentially active on this card. If MasterIntEn is also set an interrupt request is generated. Can be used for polling purposes if MasterIntEn is cleared. Interrupts can be masked with the MasterIntEn and cleared at the source in the port.

IntPortn when ‘1’ indicates there is an active interrupt request from the corresponding port. The two IntPortn signals plus ForceInt [base] are or’d together and then anded with the MasterIntEn to create the interrupt request. The corresponding port status register can be read to determine the type of interrupt being asserted.

Port Register Definitions

ChanCntl

x00 Port Control Register Port read/write

CONTROL RX	
DATA BIT	**DESCRIPTION**
31-24	spare
23	TestMode
22	FilterDefinition
21	EnableFilterInt
20	EnableFilter
19	RxOFIEn
18	RxAFIEn
17	RxIEn
16	EnableRx
15-8	spare
7	TxRdyCntl
6	TxAEIEn
5	TxIEn
4	TxStart
3	spare
2	ForceInt
1	MasterIntEn
0	ResetFifo

FIGURE 7 PMC-BISERIAL-VI-S311 PORT CONTROL REGISTER

ResetFifo when set provides a local reset to the port. The FIFO's and state-machines are reset. The registers are not reset. Return to '0' for normal operation.

MasterIntEn when '1' allows the Port interrupts to pass through to the base level of the hierarchy. When '0' the port interrupts can be polled but will not pass to the base level of the design.

ForceInt when '1' and interrupts are enabled will cause an interrupt to the base level. Useful for test and SW simulation purposes. Return to '0' to remove the interrupt request.

TxStart when '1' will start a transmission assuming that there is data in the Tx FIFO. This bit is auto-cleared when the transmission is complete

TxIEn when ‘1’ enables the Tx interrupt. The default state is off. If enabled and the master interrupt enable is enabled an interrupt is requested when the transmission is complete.

TxAEIEn when ‘1’ enables the FIFO Programmable Almost Empty interrupt. The default state is off. When enabled and the master interrupt enable is enabled an interrupt is generated when the data level falls below to the programmed level.

TxRdyCntl when ‘1’ tells the transmitter to disregard the ready signal when sending data. This allows transmitter operation when the receiver does not supply a ready output. When ‘0’ (default) the ready is required to be asserted high for transmission to occur.

EnableRx when ‘1’ allows the receive state machine to receive messages (default ‘0’).

RxIEn when ‘1’ enables the Rx interrupt to be active (default disabled). If EnableFilterInt is ‘0’, any word received will cause an interrupt, but if EnableFilterInt is ‘1’, only words whose mode bit matches FilterDefinition will cause an interrupt.

RxAFIEn when ‘1’ enables the RX FIFO Programmable Almost Full flag interrupt (default disabled). The interrupt becomes active when the data in the RX FIFO reaches a user programmed point of almost full. It requires the master enable to be asserted to create a system level interrupt.

RxOFIEn when ‘1’ enables the overflow interrupt (default disabled). The interrupt is asserted when an attempt is made to write to a full FIFO. It requires the master interrupt enable to be asserted to create a system level interrupt.

EnableFilter when ‘1’ enables data filtering. Only words with the appropriate mode bit value will be stored (default disabled). See FilterDefinition.

EnableFilterInt when ‘1’ enables the filter interrupt when the appropriate mode bit is seen (default disabled). The rx_int bit must also be set to generate an interrupt.

FilterDefinition defines what mode bit value satisfies the filter test. When ‘1’, words with mode bit = ‘1’ satisfy the test, when ‘0’ (default), words with mode bit = ‘0’ satisfy the test.

TestMode when ‘1’ selects the PCI bus as the data source for Rx FIFO writes. Normally set to ‘0’ (default). Set to ‘1’ for FIFO loop-back.

ChanStatus

x04 Port Status

Data Bit	Status	
15	int_request	1 = interrupt request after int_en mask
14	frx_ff	1 = rx fifo full, 0 = not full
13	frx_faf	1 = almost full, 0 = not almost full
12	frx_mt	1 = rx fifo empty, 0 = not empty
11	spare	
10	ftx_ff	1 = tx fifo full, 0 = not full
9	ftx_fae	1 = almost empty, 0 = not almost empty
8	ftx_mt	1 = tx fifo empty, 0 = not empty
7-6	spare	
5	TxFifoDataRdy	1 = Tx FIFO data ready for read-back
4	rx_ovfl_int	1 = receive overflow condition has been met
3	rx_int	1 = receive interrupt condition has been met
2	tx_int	1 = transmit interrupt condition has been met
1	faf_int	1 = rx almost full interrupt condition has been met
0	fae_int	1 = tx almost empty interrupt condition has been met

FIGURE 8 PMC-BISERIAL-VI-S311 PORT STATUS REG

Int_request when ‘1’ indicates that at least one of the maskable interrupts is active and enabled.

Fae_int when ‘1’ indicates that the Tx FIFO went from not almost empty to almost empty. This is a sticky bit. Clear by writing with a ‘1’ in the corresponding bit location.

Tx_int when ‘1’ indicates the transmit state machine completed sending a message. This is a sticky bit. Clear by writing with a ‘1’ in the corresponding bit location.

Rx_ovfl_int when ‘1’ indicates that an attempt was made to write data to a full Rx FIFO. This is a sticky bit. Clear by writing with a ‘1’ in the corresponding bit location.

Faf_int when ‘1’ indicates that the Rx FIFO went from not almost full to almost full. This is a sticky bit. Clear by writing with a ‘1’ in the corresponding bit location.

Rx_int when ‘1’ indicates that a word was received with the appropriate mode bit (as defined by filter_def). If filter_en is ‘0’ then any word received will cause this bit to be asserted. This is a sticky bit. Clear by writing with a ‘1’ in the corresponding bit location.

TxFifoDataRdy when ‘1’ indicates that a word is ready to read. Used for Transmission FIFO read-back. This is a sticky bit. Clear by writing with a ‘1’ in the corresponding bit location. Note: reading the Tx FIFO removes the data – no longer available to transmit.

The FIFO flags are active high. When the empty bit is high, then the FIFO is empty. When the empty flag is low, then the FIFO has at least one piece of data stored. When the Full Flag is set high, the FIFO is full. When not set, then the FIFO still has room.

ChanWordCnt

x08 Received Word Count

Data Bit	Definition
15-0	received word count

FIGURE 9 PMC-BISERIAL-VI-S311 RECEIVED WORD COUNT

WORD_CNT 15-0 is the cumulative number of words received. The count is updated as each word is stored in the receive FIFO. The count is cleared when the receiver is disabled or when a write is performed to this register address (write data value is irrelevant). After the count has been cleared, the old count will be returned when this register is read until a new word is received, beginning a new count. The Port Reset command will reset the holding register as it resides within the Rx State Machine.

ChanTxFifo

x0C TX FIFO read/write port

The BISERIAL supports 32-bit writes to the transmit data FIFO although only 18 bits are actually transmitted with the S-311 protocol. Data is aligned D31-0. Normally this port is only written to.

For loop-back testing the contents of the FIFO can be read from the “Xilinx” side of the FIFO. Once data is read from the FIFO it is no longer available for transmission. See the PreReadTxFifo register definition and Status Register bit definitions.

ChanRxFifo

x10 RX FIFO read/write port

The BISERIAL supports 32-bit reads from the receive data FIFO although only 18 bits are received with the S-311 protocol. Data is aligned D31-0. Normally this port is only read. For loop-back testing the contents of the FIFO can be written through the “Xilinx” side of the FIFO. The TestMode bit must be set to cause the PCI bus to be selected as the data source.

ChanFifoLvl

x14 FIFO level definition Port [read/write]

CONTROL REGISTER FIFO Level

DATA BIT	DESCRIPTION
31-16	PAF
15-0	PAE

FIGURE 10 PMC-BISERIAL-VI-S311 FIFO LEVEL REGISTER

PAF and PAE are written with the definitions for the Programmable Almost Full and Programmable Almost Empty levels. The Current FIFO’s are 4Kx32 which corresponds to 11-0 for the range.

Set the PAE to the count below which the PAE status is triggered. Setting to x10 means a Tx FIFO Level of x9 or less will be “true” x10 or more will be “false”.

Set the PAF to the count above which the PAF status is triggered. Setting to xFF0 means a Rx FIFO Level of xFF1 or more will be “true” xFF0 or less will be “false”.

Set the levels based on the system time to respond to the interrupt and the rate of transmission/reception.

PreReadTxFifo

x18 TX FIFO Data Request Port [write only]

CONTROL REGISTER FIFO Level	
DATA BIT	**DESCRIPTION**
31-0	Don't Care

FIGURE 11 PMC-BISERIAL-VI-S311 TX FIFO PRE-READ

The Tx FIFO transmitter port operates at the programmed Tx rate. Since this rate can be very slow compared to the PCI clock the read back method for the Transmit FIFO is as follows: 1. Write any pattern to this register. 2. Poll the Tx FIFO Data Rdy bit in the status register. When set, clear the bit. 3. Read the Tx FIFO Data from the holding register [ChanTxFIFO] Note: Tx Start must not be set or data written to the FIFO will be transmitted and not available for loop-back.

ChanTerm

x1C Termination definition Port [read/write]

CONTROL REGISTER FIFO Level

DATA BIT	DESCRIPTION
31-12	Spare
11	TermRxRdy
10	TermRxRqst
9	TermRxClk
8	TermRxData
7	TermTxRdy
6	TermTxRqst
5	TermTxClk
4	TermTxData
3-1	Spare
0	TermRefClk

FIGURE 12 PMC-BISERIAL-VI-S311 PORT TERMINATION REGISTER

The PMC-BISERIAL-VI-S311 design sets the direction of all signals in the VHDL. The terminations can be programmed. Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated. In some cases it will make sense to terminate the lines in the cable and in others, it will make sense to use the onboard terminations.

Set each of the corresponding bits to enable the termination on that line. Normally received signals are terminated and transmitted signals are terminated at the far end. It is recommended to set the bits corresponding to the RefClk, RxData, RxClk, RxRqst, TxRdy. Your system may required different settings.

ChanFifoCnt

x20 FIFO countl definition Port [read/write]

CONTROL REGISTER FIFO Count	
DATA BIT	**DESCRIPTION**
31-16	RxFifoCnt
15-0	TxFifoCnt

FIGURE 13 PMC-BISERIAL-VI-S311 FIFO COUNT REGISTER

Read the current amount of data stored in the Rx and TX FIFO's from this port. Reading the count does not affect the contents of the FIFO.

Interrupts

PMC-BISERIAL-VI-S311 interrupts are treated as auto-vectored. When software enters into an exception handler to deal with a PMC-BiSerial-VI interrupt the software must read the interrupt status to determine the cause(s) of the interrupt, clear the interrupt condition(s) and process accordingly.

The PMC-BISERIAL-VI-S311 Tx state machine generates an interrupt request when a transmission is complete and the interrupt enable bit in the control register is set. The transmission is considered complete when the Tx start bit is cleared.

The interrupt is mapped to INTA on the PMC connector. INTA may be mapped to a different interrupt in your system. The source of the interrupt is obtained by reading base status register to determine which port if any caused the interrupt [could be a shared interrupt in some systems]. Next the appropriate port status is read to determine the type of interrupt to be serviced. The interrupt can be cleared and control passed back to the operational code. The status remains valid until the status register is written with the appropriate bit.

The interrupt level seen by the CPU is determined by the rest of the system. The master interrupt can be disabled or enabled through the Bases and Channel port control registers. Both need to be enabled to pass through to the system. The individual enables for the various interrupt conditions are controllable through the port control register. This configuration allows any combination of polled and interrupt driven operation.

The individual enables operate after the interrupt holding latch, which stores the status for the CPU. Once the interrupt request is set, the way to clear the request is to write the proper bit to the interrupt status/clear register, assuming the original cause is no longer in effect or disable the master interrupt enable. The master enable is a mask and can be used to disable the interrupt from reaching the CPU, but still leaves the internal interrupt request hardware active, which is useful for polled operation.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled and the Tx, and programmable level interrupts enabled as needed. When bis_stat0 shows an interrupt pending, the appropriate action can be taken, if any, to remove the interrupt condition. Then the appropriate bit is written to the interrupt status/clear register to clear the request.

If interrupt driven the normal sequence to service an interrupt is to disable the

master interrupt enable, then read the interrupt status/clear register to determine the cause of the interrupt. If an almost full or empty interrupt has occurred, the appropriate FIFO is read or written and the appropriate bit is then written to the stat0 register, which will clear only that bit and insure that interrupt conditions will not be missed. The master interrupt enable is once again asserted and the system is ready to capture the next interrupt event.

Power on initialization will provide a cleared interrupt request and interrupts disabled.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires and external cable with the following pins connected.

Port0

Data+	7 - 22
Data-	41 - 56
Clk+	9 - 24
Clk-	43 - 58
Request+	11 - 21
Request-	45 - 55
Ready+	12 - 26
Ready -	46 – 60

Port1

Data+	14 - 29
Data-	48 - 63
Clk+	15 - 30
Clk-	49 - 64
Request+	16 - 31
Request-	50 - 65
Ready+	17 - 32
Ready -	51 - 66

In Addition add 10 MHz or similar reference to IO(0)1,35 – Port 0 RefClk and IO(1)2,36 Port 1 RefClk to allow software selection of the external reference clock.

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BiSerial-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V[unused]	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 14 PMC-BISERIAL-VI PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BiSerial-IO. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V[unused]		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 15 PMC-BISERIAL-VI PN2 INTERFACE

BiSerial-S311 Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-BiSerial-VI. Also, see the User Manual for your carrier board for more information.

IO_0p RefClk0p	IO_0m RefClk0m	1	35
IO_1p RefClk1p	IO_1m RefClk1m	2	36
IO_2p	IO_2m	3	37
IO_3p	IO_3m	4	38
IO_4p	IO_4m	5	39
IO_5p	IO_5m	6	40
IO_6p TxData0p	IO_6m TxData0m	7	41
IO_7p	IO_7m	8	42
IO_8p TxClk0p	IO_8m TxClk0m	9	43
IO_9p	IO_9m	10	44
IO_10p TxRqst0p	IO_10m TxRqst0m	11	45
IO_11p RxRdy0p	IO_11m RxRdy0m	12	46
IO_12p	IO_12m	13	47
IO_13p TxData1p	IO_13m TxData1m	14	48
IO_14p TxClk1p	IO_14m TxClk1m	15	49
IO_15p TxRqst1p	IO_15m TxRqst1m	16	50
IO_16p TxRdy1p	IO_16m TxRdy1m	17	51
IO_17p	IO_17m	18	52
IO_18p	IO_18m	19	53
IO_19p	IO_19m	20	54
IO_20p RxRqst0p	IO_20m RxRqst0m	21	55
IO_21p RxData0p	IO_21m RxData0m	22	56
IO_22p	IO_22m	23	57
IO_23p RxClk0p	IO_23m RxClk0m	24	58
IO_24p	IO_24m	25	59
IO_25p TxRdy0p	IO_25m TxRdy0m	26	60
IO_26p	IO_26m	27	61
IO_27p	IO_27m	28	62
IO_28p RxData1p	IO_28m RxData1m	29	63
IO_29p RxClk1p	IO_29m RxClk1m	30	64
IO_30p RxRqst1p	IO_30m RxRqst1m	31	65
IO_31p RxRdy1p	IO_31m RxRdy1m	32	66
IO_32p	IO_32m	33	67
IO_33p	IO_33m	34	68

FIGURE 16 PMC-BISERIAL-VI-S311 FRONT PANEL INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC-BiSerial-VI Module routed to Pn4. Also, see the User Manual for your carrier board for more information. Please note the Bezel IO is Standard [Default] add the –RIO option to the Part Number for Pn4 IO.

IO_0p	RefClk0p	IO_0m	RefClk0m	1	3
IO_1p	RefClk1m	IO_1m	RefClk1m	2	4
IO_2p		IO_2m		5	7
IO_3p		IO_3m		6	8
IO_4p		IO_4m		9	11
IO_5p		IO_5m		10	12
IO_6p	TxData0p	IO_6m	TxData0m	13	15
IO_7p		IO_7m		14	16
IO_8p	TxClk0p	IO_8m	TxClk0m	17	19
IO_9p		IO_9m		18	20
IO_10p	TxRqst0p	IO_10m	TxRqst0m	21	23
IO_11p	RxRdy0p	IO_11m	RxRdy0m	22	24
IO_12p		IO_12m		25	27
IO_13p	TxData1p	IO_13m	TxData1m	26	28
IO_14p	TxClk1p	IO_14m	TxClk1m	29	31
IO_15p	TxRqst1p	IO_15m	TxRqst1m	30	32
IO_16p	TxRdy1p	IO_16m	TxRdy1m	33	35
IO_17p		IO_17m		34	36
IO_18p		IO_18m		37	39
IO_19p		IO_19m		38	40
IO_20p	RxRqst0p	IO_20m	RxRqst0m	41	43
IO_21p	RxData0p	IO_21m	RxData0m	42	44
IO_22p		IO_22m		45	47
IO_23p	RxClk0p	IO_23m	RxClk0m	46	48
IO_24p		IO_24m		49	51
IO_25p	TxRdy0p	IO_25m	TxRdy0m	50	52
IO_26p		IO_26m		53	55
IO_27p		IO_27m		54	56
IO_28p	RxData1p	IO_28m	RxData1m	57	59
IO_29p	RxClk1p	IO_29m	RxClk1m	58	60
IO_30p	RxRqst1p	IO_30m	RxRqst1m	61	63
IO_31p	RxRdy1p	IO_31m	RxRdy1m	62	64

FIGURE 17 PMC-BISERIAL-VI-S311 PN4 INTERFACE

Applications Guide

Interfacing

The pinout tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC-BiSerial when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. PMC-BiSerial-VI does contain special input protection – TVS 400W devices on each IO for the bezel path. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the BiSerial pin definitions. It is suggested that 100 ohm twisted pair be used for your cable.

Terminal Block. We offer a high quality 68 screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68
[http://www.dyneng.com/HDEterm68.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485/LVDS devices rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BiSerial-VI is constructed out of 0.062 inch thick high temperature RoHS compliant material.

Through hole and surface mounting of components are used.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BISERIAL design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create high power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options. http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Host Interface:	PCI Mezzanine Card
Serial Interface:	RS-485 Tx_Data, Tx_Clk, Tx_Request, Rx_Ready, Rx_Data, Rx_Clk, Rx_Request, Tx_Ready, REFCLK
TX CLK rates generated:	12 bit divisor with 10 MHz, 33/2 MHz. and REFCLK input rates. Other rates available with special oscillator installation
Software Interface:	Control Registers, Status Ports, FIFO
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Interrupt:	All Programmable. Tx interrupt at end of transmission Programmable Almost Empty Programmable Almost Full Rx Overflow Configurable Rx interrupt
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module.
Construction:	Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	0.89 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC-BISERIAL-IO-S311	PMC Module with 2 Tx and 2 Rx serial channels, Programmable data rates Special protocol support, RS-485 drivers and receivers 32 bit data interface Industrial Temperature standard
-RIO	Remove Bezel and add Pn4 IO
-ROHS	Change from standard to RoHS assembly
-CC	Add Conformal Coating

Other Related Options:

HDEterm68	68 position screw terminal adapter Options for DIN rail mounting, SCSI connector orientation, incorporates reference plane, differential routing.
HDEcabl68	SCSI type 68 IO twisted pair cable