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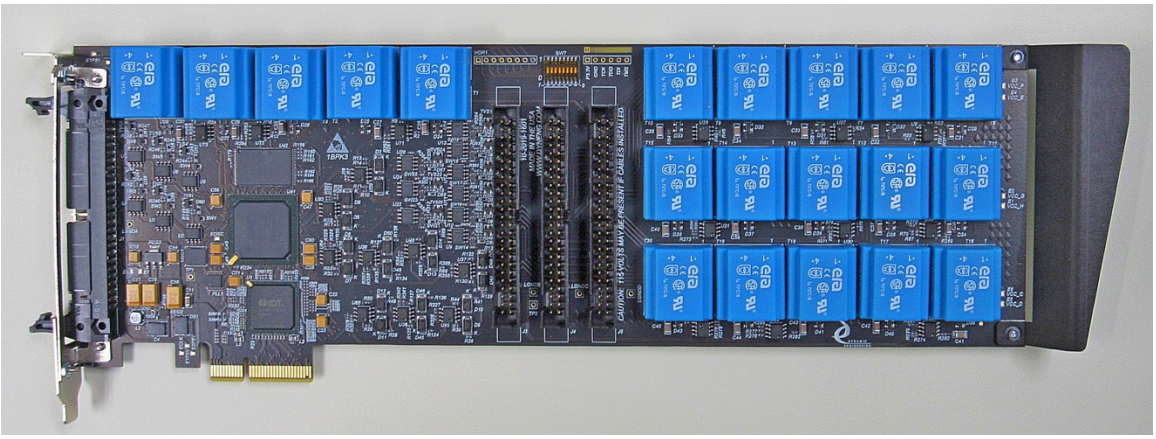
Est. 1988

User Manual

PCIe-Harpoon



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PCIe-HARPOON

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Connection of incompatible hardware is likely to cause serious damage.

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Product Description

PCIe-HARPOON is part of the Dynamic Engineering PCIe compatible family of modular I/O components. PCIe-HARPOON provides an FPGA based interface to provide 4 ports with 28V inputs, High Side Switches, Low Side Switches, 115V detection and Differential IO. PCIe-Harpoon is a direct update for PCI-Harpoon – in service since 2008. The design is updated to the PCIe bus, new right-angle bezel connector, updated components, industrial temperature etc.

Special features:
- PCIe compliant
- 4 ports
- DIP Switch for user configuration control
- 5 Optically Isolated [7V-28V] inputs plus 2 power monitors per port
- 7 High Side Switches per port
- 4 Low Side Switches per port
- 6 Differential IO per port
- 5 115V sense circuits per port
- JTAG programming support
- Options for DMA and alternate IO implementations

The four IO ports each have a separate 50 pin header. Ribbon or discrete wiring cables can be installed. Port 0 is closest to the bezel and has a right-angle connector installed for external cable connections. The remaining ports 1-3 will require internal to external cabling. PCIe-Harpoon features a special cable bezel with room for the 3 internal ports to pass through the bezel in addition to the right-angle port 0 connector. The internal headers are non-ejector types standard to meet PCI/PCIe height requirements. The connectors can be replaced with ejector types if desired.

HDRribn50 plus HDRterm50 can be utilized as a breakout : http://www.dyneng.com/HDRribn50.html The ribbon cable is available in standard and custom lengths. HDRterm50 is a screw terminal break-out for ribbon cable and other cabling systems utilizing 50 pin headers. The breakout can provide an easy adapter between system discrete wiring requirements, and the 50 pin headers used on PCIe-HARPOON. http://www.dyneng.com/HDRterm50.html Please contact Dynamic Engineering with your requirements.

An 8 position DIP Switch is provided. The DIP Switch is connected to the FPGA and can be read through a status port. When multiple PCIe-HARPOON devices are

installed within a system the DIP Switch can be read to determine which PCIe Addresses go with each set of external connections.

28V inputs are provided using “optoiso” components.

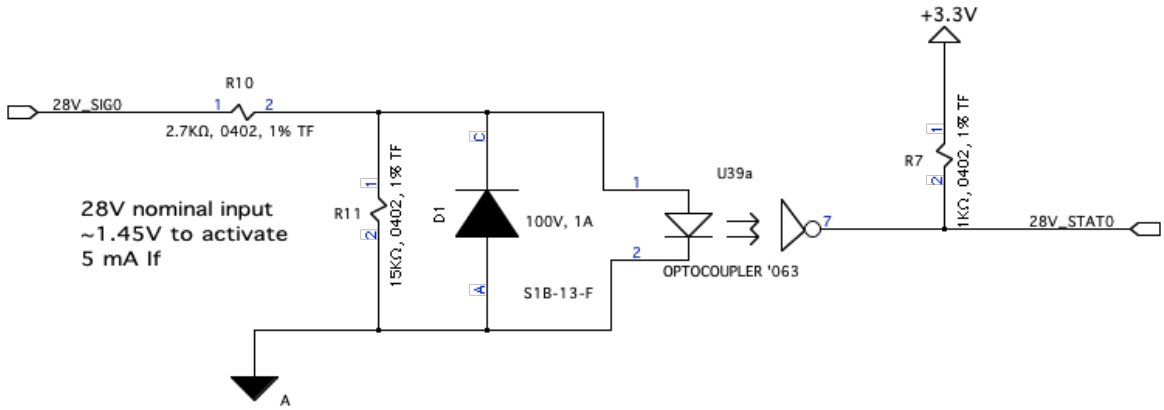

FIGURE 1 PCIE-HARPOON OPTOISO CKT

Each port has five 28V inputs. The standard values will provide true status for 7V – 28V signals. Higher and lower voltages can be accommodated by altering the series resistor to limit the current through the isolation component. The 28V input is referenced to a ground associated with that port. The FPGA inverts and presents the status of the lines in the PCIe-HARPOON design. Additional processing can be added for designs with alternate requirements.

The High Side switches are for the purpose of switching power on and off under software control. Each channel has two independent reference voltages. The High Side Switches provide software control of these voltages.

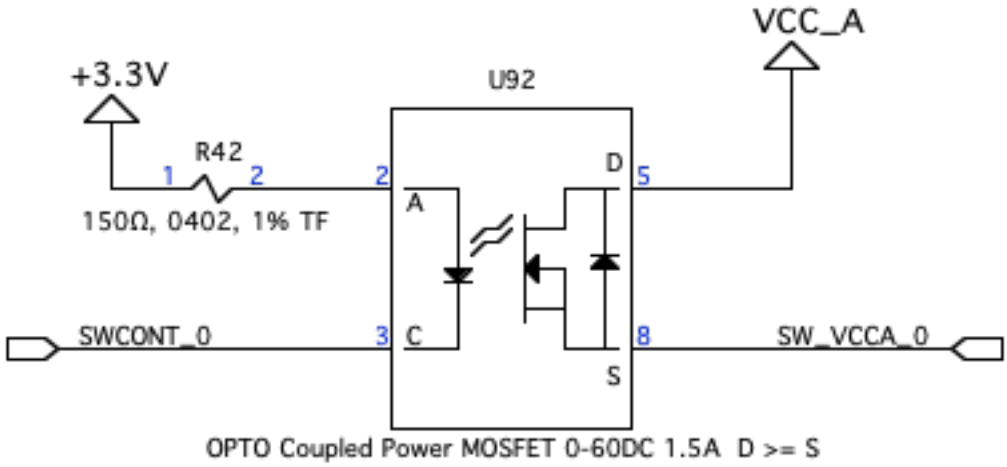

FIGURE 2 PCIE-HARPOON HIGH SIDE SWITCH CKT

Each port has 7 of the above circuits. 5 are referenced to one voltage and two to the alternate voltage on each channel. The outputs are controlled with registers instantiated within the FPGA for the PCIe-HARPOON design. The outputs could be based on a state-machine or other logic interacting with the 28V inputs if desired.

The Low Side Switches are similar to the High Side, and for the purpose of switching ground. Due to the topology of the FET the Source side is tied to the common ground and the Drain is connected to the external circuit. The reference ground is the channel ground. There are 4 Low Side Switches per channel.

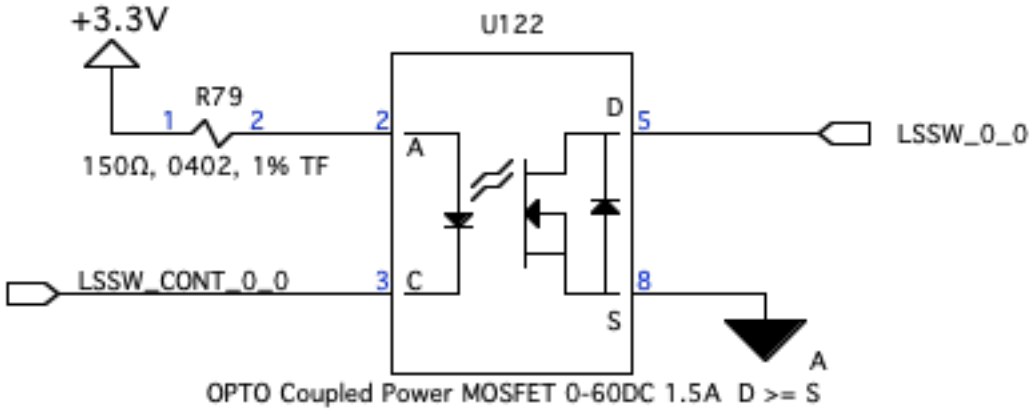

FIGURE 3 PCIE-HARPOON LOW SIDE SWITCH CKT

The grounds can be made common by tying together externally. The VCC references can also be made common by external connection.

The 115V sense circuits are designed to check if a 115V AC signal is present. The AC voltage is not specifically measured, rather a transformer reduced and rectified version is tested. The follow circuit shows a typical single-phase circuit.

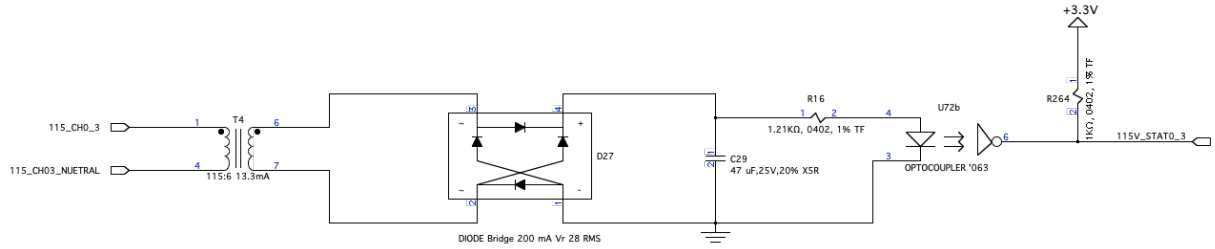

FIGURE 4 PCIE-HARPOON 115V STATUS CKT

There are 2 single phase circuits and 1 - 3 phase circuit per channel. The 3-phase circuit has a common neutral, and is otherwise the same as the single phase circuits. The 115V is reduced with a transformer, rectified with a bridge and capacitor, and tested with an optically isolated gate. The capacitor is sized to hold a DC level for the optoiso receiver. The status will be on or off. If the capacitor is reduced in value the voltage can switch with the AC cycle to allow frequency measurements. The current limit resistor protects the optoiso receiver.

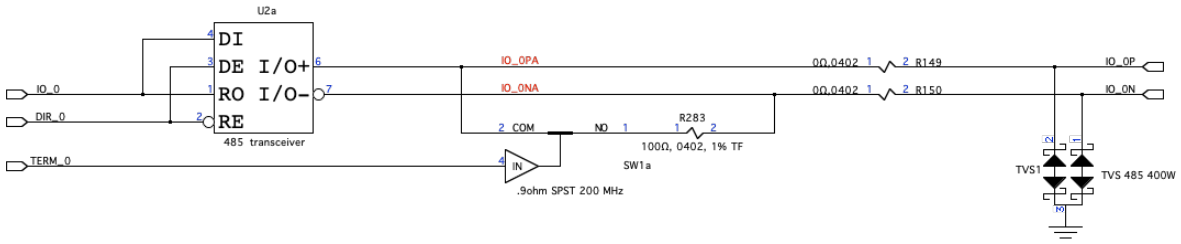

FIGURE 5 PCIE-HARPOON DIFFERENTIAL IO CKT

Each of the ports has 6 differential IO. Each IO has a transceiver with RS-485 protocol, an analog switch plus termination resistor, and optional IO termination resistors. The transceivers each have separate direction controls. The parallel terminations are individually programmable. Each port has TVS protection.

The transceivers are used to implement a serial protocol for PCIe-HARPOON. The serial interface receives clock, data and an enable to control the receiving of data. Data is transmitted from PCIe-HARPOON in parallel with receiving a word.

The master interface sends commands to the target. Some are writes and some require data to be returned. When a read command occurs the data is returned on the next command – pipeline fashion. The n-1 transfer response is expected on the nth transfer. Interrupts are provided to support fast response to the received data.

PCIe-HARPOON incorporates a test clock and enable to be used for loop-back testing. When interconnected externally the test clock becomes the receive clock and the test enable becomes the receive enable. Data out becomes data in. To support more complete testing an optional inverter can be enabled to make the received data the inverse of the transmitted data.

Two interrupts are available per port. The Tx and Rx interrupts indicate the respective processes are complete in HW. Generally the Rx interrupt will be used due to the nature of the interface with Rx required to create Tx.

Data is transmitted with the data sent LSB first, Parity last with 16 data bits for a 17 bit transmit length. Data is valid on the falling edge, and clocked out on the rising edge of the clock. The clock is low between transfers. Enable is active high.

The base rate for the PCIe-Harpoon interface is ~100 KHz. The transceivers are rated at 50 MHz. The board routing is matched length between each of the 6 IO per channel.

The clock rate is based on the external PLL. The rate can be changed with software. The driver sets the base rate and can be used to change to alternate frequencies. The default rate is automatically loaded by the driver. New frequencies can be loaded with the utilities included in the SW packages.

Each port has 6 IO. The IO are numbered 0-5 in the pinout table. The correspondence is as follows for PCIe-Harpoon IO.

RX Enable	IO_0
RX Clock	IO_1
RX Data	IO_2
TX Enable [for master or loop-back only]	IO_3
TX Clock [for master or loop-back only]	IO_4
TX Data	IO_5

FIGURE 6 PCIE-HARPOON SERIAL IO DEFINITIONS

The FPGA is loaded at power up from FLASH memory. The FLASH memory is programmed at Dynamic Engineering using the JTAG header located at the top center of the card. The JTAG header can be used in the field to update programs stored in FLASH memory. Should an update be requested or required the bit file for the FLASH can be e-mailed to the client for an “instantaneous” update.

For example, if your project requires something similar to the PCIe-Harpoon, but different in a way that can be accomplished with VHDL changes. Dynamic Engineering can send the current PCIe-HARPOON design to you and follow-up with a bit file to update the board. The name will be updated to PCIe-HARPOON-XXX to control the new version. The revision within the version is stored into the FLASH to allow software to track the hardware revisions.

A standard Xilinx serial download cable will be required [if you are making changes]. The flying lead option works best. Parallel cable IV or later is recommended. Available from the Xilinx store or we can arrange to include with your order if that is more convenient.

The FPGA is fully connected to the local PCI bus to allow for DMA processing. The base PCIe-HARPOON does not require DMA as it is essentially a single word at a time interface with host intervention – DMA does not make sense in this case. If your project has a larger data structure to pass the internal memory within the FPGA plus the Dynamic Engineering DMA engine can be used to increase performance. Please contact Dynamic Engineering for DMA or other options. The local bus can operate at 33 or 50 MHz based on resistor strap. The default is 50 MHz.

Register Map for PCIe-HARPOON

Name	Offset from Base
BASECONTROL	0x0000 // 0 Harpoon base control register
REVISION	0x0004 // 1 Harpoon ID Register
MASTINTCNTL	0x0008 // 2 Harpoon Base Master Interrupt Enable
// Port N	
CHANCONTROL	0x0000 // 0 Channel Base Register offset
CHANSTATUS	0x0004 // 1 Channel Stat28 [4-0] STAT115 [20-16]
CHANTESTSTART	0x0008 // 2 Channel test start
CHANMASTERINT	0x000c // 3 Channel Master Interrupt Enable
TXAMTCNT	0x0018 // 6 Test Register Spare
RXAFLCNT	0x001C // 7 Test Register Spare
TXRXDATA	0x0020 // 8 write TX data read RX data
CHANSWCNTL	0x0024 // 9 Low Side and High Side SW Control

The offsets shown are relative to the base address assigned by the PCI enumeration process. Channel addresses are shown as offsets from the port base. See port descriptions for the additional port addresses. Please note that the port addresses are repeated in the same order with the same offsets from their base addresses. PCI references are used as this design has a Bridge between the PCIe and local PCI bus. The FPGA sits on the PCI bus.

Port N offset = port 0 offset + (Port)N * Port size = 0x10 + (Port)N * 0x28

VendorID DCBA
DeviceID 006C

Bit Maps for PCIe-HARPOON Registers

BASECONTROL offset 0x00

Bit	Definition
20	SDATREG
19	pll_SDAT
18	reserved
17	pll_SCLK
16	pll_EN
15-0	spare

The Base register has 16 bits of unused read-write data bits reserved for future definition.

The PLL is controlled through bits 19-16 of the base register. The driver has calls available to control the PLL. The register bits for pll_Enable, pll_SCLK are unidirectional from the Xilinx to the PLL – always driven. Pll_SDAT is open drain. The SDAT register bit when written low, and enabled will be reflected with a low on the SDAT signal to the PLL. When SDAT is taken high or disabled the SDAT signal will be tri-stated by the Xilinx, and can be driven by the PLL. The SDAT register bit when read reflects the state of the SDAT signal between the Xilinx and PLL and can be in a different state than the written SDAT bit. To read back the contents of the CMD port use the SDATREG port.

PLL enable: When this bit is set to a one, SDAT is enabled. When set to '0' SDAT is tri-stated by the Xilinx.

PLL sclk/sdata output: These signals are used to program the PLL over the I2C serial interface. SCLK is always an output whereas SDAT is bi-directional.

PLL s2 output: This is an additional control line to the PLL that can be used to select additional pre-programmed frequencies.

SDATREG: is the register bit read-back for the data bit.

The PLL is a separate device controlled by the Xilinx. The PLL has a fairly complex programming requirement which is simplified by using the Cypress® frequency descriptor software, and then programming the resulting control words into the PLL using the PLL Control ports. The interface can be further simplified by using the

Dynamic Engineering Driver to take care of the programming requirements.

The PLL uses a reference clock. The reference is from the oscillator installed on the PCIe-HARPOON and fed through the Xilinx. The frequency for the reference can be altered by installing a different oscillator or by changing the VHDL – use the PCI clock as a reference for example. The oscillator is 40 MHz. The PLL reference is 20 MHz. The PLL has two outputs connected back to the FPGA. Clock A is used by the PCIe-HARPOON design to control the serial IO. The second input is spare in the PCIe-HARPOON and available for new requirements.

Please note: original design had a 40 MHz reference to PLL. Frequency files will need to be updated. Win10 SW package comes with an updated file. PCIe-Harpoon.jed.

REVISION offset 0x04

Bit	Definition
23-16	RevisionMinor
15-8	RevisionMajor
7-0	DIP Switch

The FPGA is programmed with VHDL. The revision of the design is available for software to read via the ID port.

The DIP Switch is read through the ID port. The value read corresponds to the value set on the switch. The switch has no direct effect on board performance. The setting can be used to match a particular board / cable set to a somewhat random PCI address assigned. The ability to match hardware to address is particularly useful when multiple boards are used within a system.

Revision Log: [Major.Minor]

Initial development 0101 & 0102 7/9/20

MASTERINTCNTL offset 0x08

Bit	Definition
31-28	Port Interrupt Status
27-1	Spare
0	MasterIntEn

MasterIntEn when set ‘1’ gates any of the Port Interrupt Requests to the system. When not enabled the port interrupt request status can be polled.

Port Interrupt Status bits align with ports 3-0. The interrupt handler can read this port and know if any port on the board is active. The status is read-only. Writing to the register has no effect on these bits.

CHANCONTROL offset 0x10,38,60,88

Bit	Definition
31-16	not present
15-12	Spare
11	RXTERM
10	TXTERM
9	RXINTEN
8	TXINTEN
7	RXDATINV
6	RX_EN
5	TX_EN
4	FORCEINT
3-0	Spare

All bits are R/W. PCIe-HARPOON operational bits are defined below.

RXTERM and TXTERM are used to enable or disable the programmable ~100Ω termination between the ± sides of the differential pairs. When set to '1' the termination is enabled causing the resistor to be connected between the RX or TX pair. When '0' the termination is disconnected. Typical operation would have the termination enabled on the RX and disabled on the TX. If your system has terminations in the cable, or if your system is particularly noisy, or perhaps there are no terminations at the receiving side for the transmitters on the PCIe-HARPOON; it may be necessary to use terminations on both sides or neither.

Please note : Channel and Base Master Interrupt Enables must be enabled for a ports interrupt request to reach the host. With separate enables it is possible to use polling of the interrupt status to operate or gate through to use as interrupts.

RXINTEN when set '1' gates the end of reception status to the channel interrupt level.

TXINTEN when set '1' gates the start of transmission status to the channel interrupt level.

The RX interrupt corresponds to an interrupt at the end of the Enable signal – when a complete word has been received. The TX interrupt corresponds to the leading edge of the Enable signal – when the transmission starts. Data has been loaded into the output shift register when the interrupt is set allowing the next word to be loaded should that be desired.

FORCEINT when set ‘1’ gates the User interrupt to the channel interrupt level. This function is useful for software development and for hardware test.

TX_EN when set ‘1’ allows the state-machine to transmit data when the enable and clock are received. When ‘0’ the data stored in the shift register for transmission is forced to ‘0’ before going to the transceiver. Please note that the data in the shift register is not set to ‘0’ allowing received data to be read.

RX_EN when set ‘1’ allows the state-machine to receive data using the Enable and Clock. When ’0’ the data is forced to ‘0’ prior to loading into the shift register. If used in a TX only mode the data in the SR will be ‘0’ after transmission and before reloading.

RXDATINV when set ‘1’ will cause the received data to be inverted prior to loading. RXDATINV requires RX_EN to be set. When in loop-back the received data is stored back into the same shift register that the transmit data comes from. The inversion of the received data allows the shift register data to be different from the transmit data when received to prove that the data was transmitted and received.

All undefined bits should be set to ‘0’.

Not Present bits are not implemented in HW.

CHANSTATUS offset 0x14,3C,64,8C

Bit	Definition
31	INT_STAT
30	LOC_INT
29-21	spare = 0
20-16	STAT_115V(4-0)
15-11	spare = 0
10	FORCEINT
9	RXINT
8	TXINT
7	spare = 0
6	VCC_x(A,C,E,G)
5	VCC_y(B,D,F,H)
4-0	28V_SIG(4-0)

INT_STAT when set indicates that an interrupt request is active for this port. Still requires MasterIntEn at the base level to become a Card level interrupt request.

LOC_INT when set indicates that TX, RX or FORCEINT are asserted. Status before the port level MasterIntEn gate. If the local master is enabled, INT_STAT will also be set.

INT_STAT and LOC_INT are status only – the interrupts represented are cleared by other action. Rewriting INTFORCE low for example.

RXINT and TXINT are set when the state-machine detects that the corresponding conditions have occurred. The Signals are taken before the mask is applied so the status can be used for polling if the interrupts are not actually enabled. The status is held in a latch which is cleared when written to with the corresponding bits set [write to ChStat].

28V_SIG bits 4-0 VCCx, VCCy. When a voltage in the range of 7- 28V is present on the IO or power monitoring inputs, the status bit is set. No filtering is implemented in PCIe-HARPOON. The bits are referenced to the ground associated with the port. The voltage and ground can be at different potentials than the local PCIe-HARPOON ground due to the use of an Opto-Coupler in the receiver.

STAT_115V(4-0) are set when 115V is present on the corresponding IO pin input. 0,1,2 are part of a 3-phase detector with one neutral for the three signals. There is no phase requirement for the detector on the PCIe-HARPOON to work properly. Inputs 3 and 4

support single phase measurements. All 5 inputs can be used for single phase if the neutrals are at a common potential between the first three signals to measure.

Each signal is transformer coupled and reduced by ratio. The lower voltage AC is fed through a DIODE bridge and capacitor to rectify sufficiently to make a go-nogo assessment of an AC voltage near 115 being present.

The DC voltage is optically coupled to provide safety and isolation in case of improper AC connections.

Please note that 115V power will be present at certain exposed points on the PCIe-HARPOON when 115V is attached to the IO connectors. Main points are the transformer and IO pins. Exercise appropriate caution in handling the board. Additional warnings are silk-screened front and rear of the PCB.

CHANTESTSTART offset 0x18,40,68,90

Bit	Definition
2	TEST_CNTRL_CLOCK
1	TEST_CNTRL_ENABLE
0	TEST_CNTRL_AUTO

TEST_CNTRL_AUTO When this bit is written to the port [PCIe-HARPOON-ChTS] the hardware will generate the clock, and enable signals for a standard transfer of data from the PCIe-HARPOON. The start bit is self-clearing at the end of each transfer.

TEST_CNTRL_ENABLE This bit directly controls the state of the enable_out signal.

TEST_CNTRL_CLOCK This bit directly controls the state of the clock_out signal.

If the external IO signals are looped-back to the inputs the Clock Out will become the Clock in, and the Enable Out will become the Enable in. If the RX and TX enables are set, and if data has been loaded into the shift register; the data in the shift register will be transmitted from the output data IO. If the TX data is looped-back to the RX data, a complete loop-back test can be performed.

The interrupts can be used for status. No direct read-back is supported for TS. Not used for normal operation. Can be used to cause the PCIe-HARPOON to act as a bus master on the serial bus.

CHANMASTERINT offset 0x1C, x44, x6C, x94

Bit	Definition
31-1	Spare
0	ChanMasterIntEn

ChanMasterIntEn when set ‘1’ gates any of the local Port Interrupt Requests to the Base level. When not enabled the local port interrupt request status can be polled.

Please note: two test registers are located at offsets [from channel base] x18, x1C for each port. These registers can be used for SW development and self-test. 16 bits on 32 bit boundaries.

TXRXDATA offset 0x30,58,80,A8

Bit	Definition
TX	
16-0	write to load shift register, read from shift register
RX	
16	Parity
15-0	data, bit 0 received and transmitted first, parity last

Data written to this port will be moved into the transmit / receive shift register. There is a delay in moving the data from the holding register to the shift register due to synchronizing the PCI referenced port write signal with the state-machine based shift register load signal. When the Tx interrupt status is set, new data can be written to this register.

When the RX Int status is set the received data is available to be read.

CHANSWCNTL offset 0x34,5C,84,AC

Bit	Definition
15-11	Spare
10-4	SW(6-0)
3-0	LSSW(3-0)

The High and Low side switches are controlled from this port. SW corresponds to the High Side Switches. LSSW corresponds to the Low Side Switch ports.

When set the port is active = low impedance connection and when cleared the ports are disabled. Each port has an opto-coupled FET and either a connection to the channel power supplies or to the channel ground.

Each port has a single reference ground. For example, LGND0 is the ground for port 0. When a LSSW bit is set, the corresponding FET is enabled connecting the signal tied to the Drain to the Source. The Source of the FET is tied to LGNDx.

Each port has two power supply inputs. VCC_A and VCC_B are the port 0 names. (names are the other three port names) The first 4 switches(3-0) are referenced to VCC_A(C,E,G) the next two (5,4) are referenced to VCC_B(D,F,H), and the last (6) to VCC_A(C,E,G). The Source side of the opto-FET is tied directly to the reference voltage and the drain to the IO pin.

The FET's can handle 1.5A and are rated to 60V. The traces and connector pins have similar ratings. Ribbon cable typically does not support 1.5A. Discrete wiring cables may be required for larger current requirements.

Loop-Back Testing

Dynamic Engineering uses loop-back testing to check PCIe-HARPOON for proper operation as part of our manufacturing testing. The Windows driver package software includes the application software that we use to run the tests. The software requires a test fixture to interconnect the IO and provide external references.

The test fixtures are connected to the IO connectors on PCIe-HARPOON. On each fixture the following connections are made.

1. external power supply set to 28V – connect to pins 13-18
2. external power supply ground – connect to pins 19-22
3. connect HS switch with VCCA reference to 28V inputs
   23-30
   24-31
   25-32
   26-33
   29-34
4. Use LED circuit #1 to test Low Side Switches : 28V–LED–Resistor–IO pin
   With the LEDs we use, a value of 1200-1400 ohms is appropriate
   The LED will illuminate when the Low Side Switch is enabled supplying the ground.
   Build 4 circuits and use IO pins 9,10,11,12
5. Use LED circuit #2 to test secondary High Side Switch referenced voltage
   IO Pin-Resistor-LED-Ground
   Make two circuits and tie to IO pins 27 and 28
6. Add 115V test circuit using a standard 3 prong cable.
   Tie IO pins 4,6,8 together and to the neutral [blue in our cable]
   Tie IO pins 1,2,3,5,7 to the 115 side of the power cable [brown]
   use a power strip or similar to be able to turn the 115V on and off.
7. loop-back for the serial ports – interconnect clock, data and enable
   40-46, 42-48, 44-50, 39-45, 41-47, 43-49

IO Interface Pin Assignment

The following figures give the pin assignments for the IO Interface – header pin number to signal name for the PCIe-HARPOON connectors.

Port 0

Signal Name		J2	
IO0_5N	IO0_5P	50	49
IO0_4N	IO0_4P	48	47
IO0_3N	IO0_3P	46	45
IO0_2N	IO0_2P	44	43
IO0_1N	IO0_1P	42	41
IO0_0N	IO0_0P	40	39
GND	GND	38	37
GND	GND	36	35
28V_SIG0_4	28V_SIG0_3	34	33
28V_SIG0_2	28V_SIG0_1	32	31
28V_SIG0_0	SW_VCCA_4	30	29
SW_VCCB_1	SW_VCCB_0	28	27
SW_VCCA_3	SW_VCCA_2	26	25
SW_VCCA_1	SW_VCCA_0	24	23
LGND0	LGND0	22	21
LGND0	LGND0	20	19
VCC_B	VCC_B	18	17
VCC_A	VCC_A	16	15
VCC_A	VCC_A	14	13
LSSW_0_3	LSSW_0_2	12	11
LSSW_0_1	LSSW_0_0	10	9
115_CH04_NUETRAL	115_CH0_4	8	7
115_CH03_NUETRAL	115_CH0_3	6	5
115_CH0_NUETRAL	115_CH0_2	4	3
115_CH0_1	115_CH0_0	2	1

FIGURE 7 PCIE-HARPOON J2 CONNECTOR PIN DEFINITION

J2 is provided standard with a right angle connector. Pin one is marked with the J# on the slk-screen and a square pad. Standard numbering patterns are used. J# pin numbering in the chart is in the same relative positions as the top view of the connector on the PCB.

LGND0 is the reference for both VCC_A and VCC_B. LGND0 is also used as the reference for the 28V signals [28V_SIG0_X].

Port 1

Signal Name		J3	
IO1_5N	IO1_5P	50	49
IO1_4N	IO1_4P	48	47
IO1_3N	IO1_3P	46	45
IO1_2N	IO1_2P	44	43
IO1_1N	IO1_1P	42	41
IO1_0N	IO1_0P	40	39
GND	GND	38	37
GND	GND	36	35
28V_SIG1_4	28V_SIG1_3	34	33
28V_SIG1_2	28V_SIG1_1	32	31
28V_SIG1_0	SW_VCCC_4	30	29
SW_VCCD_1	SW_VCCD_0	28	27
SW_VCCC_3	SW_VCCC_2	26	25
SW_VCCC_1	SW_VCCC_0	24	23
LGND1	LGND1	22	21
LGND1	LGND1	20	19
VCC_D	VCC_D	18	17
VCC_C	VCC_C	16	15
VCC_C	VCC_C	14	13
LSSW_1_3	LSSW_1_2	12	11
LSSW_1_1	LSSW_1_0	10	9
115_CH14_NUETRAL	115_CH1_4	8	7
115_CH13_NUETRAL	115_CH1_3	6	5
115_CH1_NUETRAL	115_CH1_2	4	3
115_CH1_1	115_CH1_0	2	1

FIGURE 8 PCIE-HARPOON J3 CONNECTOR PIN DEFINITION

J3 is provided standard with a vertical connector. Pin one is marked with the J# on the slk-screen and a square pad. Standard numbering patterns are used. J# pin numbering in the chart is in the same relative positions as the top view of the connector on the PCB.

LGND1 is the reference for both VCC_C and VCC_D. LGND1 is also used as the reference for the 28V signals [28V_SIG1_X].

Port 2

Signal Name		J4	
IO2_5N	IO2_5P	50	49
IO2_4N	IO2_4P	48	47
IO2_3N	IO2_3P	46	45
IO2_2N	IO2_2P	44	43
IO2_1N	IO2_1P	42	41
IO2_0N	IO2_0P	40	39
GND	GND	38	37
GND	GND	36	35
28V_SIG2_4	28V_SIG2_3	34	33
28V_SIG2_2	28V_SIG2_1	32	31
28V_SIG2_0	SW_VCCE_4	30	29
SW_VCCF_1	SW_VCCF_0	28	27
SW_VCCE_3	SW_VCCE_2	26	25
SW_VCCE_1	SW_VCCE_0	24	23
LGND2	LGND2	22	21
LGND2	LGND2	20	19
VCC_F	VCC_F	18	17
VCC_E	VCC_E	16	15
VCC_E	VCC_E	14	13
LSSW_2_3	LSSW_2_2	12	11
LSSW_2_1	LSSW_2_0	10	9
115_CH24_NUETRAL	115_CH2_4	8	7
115_CH23_NUETRAL	115_CH2_3	6	5
115_CH2_NUETRAL	115_CH2_2	4	3
115_CH2_1	115_CH2_0	2	1

FIGURE 9 PCIE-HARPOON J4 CONNECTOR PIN DEFINITION

J4 is provided standard with a vertical connector. Pin one is marked with the J# on the slk-screen and a square pad. Standard numbering patterns are used. J# pin numbering in the chart is in the same relative positions as the top view of the connector on the PCB.

LGND2 is the reference for both VCC_E and VCC_F. LGND2 is also used as the reference for the 28V signals [28V_SIG2_X].

Port 3

Signal Name		J5	
IO3_5N	IO3_5P	50	49
IO3_4N	IO3_4P	48	47
IO3_3N	IO3_3P	46	45
IO3_2N	IO3_2P	44	43
IO3_1N	IO3_1P	42	41
IO3_0N	IO3_0P	40	39
GND	GND	38	37
GND	GND	36	35
28V_SIG3_4	28V_SIG3_3	34	33
28V_SIG3_2	28V_SIG3_1	32	31
28V_SIG3_0	SW_VCCG_4	30	29
SW_VCCH_1	SW_VCCH_0	28	27
SW_VCCG_3	SW_VCCG_2	26	25
SW_VCCG_1	SW_VCCG_0	24	23
LGND3	LGND3	22	21
LGND3	LGND3	20	19
VCC_H	VCC_H	18	17
VCC_G	VCC_G	16	15
VCC_G	VCC_G	14	13
LSSW_3_3	LSSW_3_2	12	11
LSSW_3_1	LSSW_3_0	10	9
115_CH34_NUETRAL	115_CH3_4	8	7
115_CH33_NUETRAL	115_CH3_3	6	5
115_CH3_NUETRAL	115_CH3_2	4	3
115_CH3_1	115_CH3_0	2	1

FIGURE 10 PCIE-HARPOON J5 CONNECTOR PIN DEFINITION

J5 is provided standard with a vertical connector. Pin one is marked with the J# on the slk-screen and a square pad. Standard numbering patterns are used. J# pin numbering in the chart is in the same relative positions as the top view of the connector on the PCB.

LGND3 is the reference for both VCC_G and VCC_H. LGND3 is also used as the reference for the 28V signals [28V_SIG3_X].

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
The PCIe-HARPOON may need to be mounted with the system cables prior to installation within the chassis. The rear of the board is fitted with an offset rail that will align with the chassis card guide. The front of the card has a bezel that should be mounted to the chassis and retained with a screw.

The system cables can be routed out of the chassis. Port 0 is available directly with the right angle trough the bezel connector. Ports 1,2 and 3 cables can be routed through the bezel by use of the cable slot built into the bezel. The bezel has a special feature, loosen the retaining screw and pivot the cable retainer out of the way. Lay the flat cables into the slot. Return the retainer and retighten. The metal is thin ⇔ be careful not to over torque to prevent damage. As you install PCIe-Harpoon with cables attached, pass the cables through the chassis bezel and then seat the card while continuing to move the card into position. Sounds complex but is easier than it appears.

If using discrete wiring it may be too thick to use the bezel slot at least for all three. Adjacent bezel openings can be used in this case.

The PCIe-HARPOON has 115V detectors. The card does not generate 115V, but will have 115V present if the detectors are connected to 115V sources. Be Careful handling the card and cables when 115V is present.

The PCIe-HARPOON is a rugged card with modern electronics installed. ESD handling procedures need to be followed to prevent damage to the card.

The silk-screen indicates the ESD handling and 115V safety requirements.

Start-up
Make sure that the "system" can see your hardware before trying to access it. In Windows systems the Device Manager can be used. In Linux LSPCI is effective.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

The PCIe-HARPOON can handle multiple different ground points – one per channel. Please be careful to use the correct ground for the correct channel. Multiple channels can be interconnected – ground – to use a common reference.

The PCIe-HARPOON has multiple reference input power supplies which can be left separate or tied together in many combinations. The reference ground for the channel must be associated the reference power used on that channel.

Construction and Reliability

PCIe-HARPOON is constructed out of 0.062 inch thick High temp ROHS compliant FR4 material.

PCIe-HARPOON is a full length PCIe board. The width and height are compliant. The front side max component height is .473". The rear max component height is .195". The PCI/PCIe specification allows .570" front size and .105" on the rear side. The PCIe-HARPOON is within the standard on the front side. There is a minimum of .051" air gap in the PCIe specification, meaning that the Harpoon is .039" into the next card's space to the rear.

Multiple Harpoon's can be installed back-to-back. If the next card is .530" or less no interference will result on the back side. Most card designs do not come to the limit of the front side height.

Thermal Considerations

The circuitry in use on the PCIe-HARPOON is low power. Under normal circumstances the standard cooling within a PC will be adequate to cool the board.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
InterNet Address support@dyneng.com

Specifications

Logic Interfaces:	PCIe 4 lane Gen1, local PCI 33 or 50 MHz w/ 32 bit data bus
Access types:	LW based design
Channels	4 ports per PCIe-HARPOON
CLK rates supported:	programmable via PLL. Base rate of 100 KHz. for serial IF
28V Inputs	5 plus 2 power monitor per port [status true 7V-28V]
Low Side Switch	4 per port [1.5A max]
High Side Switch	7 per port [1.5A, 60V max]
Serial Interface	Data, Clock, Enable RX/TX interface RS-485
Software Interface:	register mapped
Initialization:	software control over all options
Interface:	50 pin header per channel
Dimensions:	full length PCIe board, single PCIe slot width not accounting for cabling
Construction:	High Temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.

Order Information

Industrial temperature range components -40⇔85ºC

PCIe-HARPOON	Full length PCIe card with 4 ports 28V Inputs(7), HS Switches(7), LS Switches(4), serial interface per port
-ROHS	Add ROHS compliant processing
-CC	Add conformal coating
HDRterm50	www.dyneng.com/HDRterm50.html 50 pin Header to 50 screw terminal with DIN rail mounting.
HDRribn50	www.dyneng.com/HDRribn50.html 50 pin ribbon cable.
IP-Debug-IO	www.dyneng.com/ipdbgio.html 50 pin ribbon to header adapter with IP connector. Can be used for loop-back with this design. HDRterm50 can also fill this role.