DYNAMIC ENGINEERING

User Manual

PCI3IP-Minimap

PCI 3 Slot IP Compatible Carrier
2KB Address Space

Manual Revision A
Corresponding Hardware: Revision 3
Corresponding Firmware Revision A
10-1999-0403

PCI3IPmm
PCI based IP Compatible Carrier

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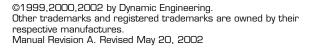Connection of incompatible hardware is likely to cause serious damage.

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Product Description

PCI3IPmm is part of the IP Compatible family of modular I/O components. The PCI3IPmm provides three IndustryPack Compatible sites in one PCI slot.

ID, IO, INT, and MEM access types are supported for read and write cycles. All four spaces are limited to 128 bytes to provide a minimum address space for systems with limited memory.

The PCI bus is 32 bits wide and most industry packs are 16 bit devices. Byte, word, and long word accesses are supported. Bytes can be to any address. Word accesses need to be word aligned. Long word accesses need to be long word aligned. Each of the access types has a one-to-one correspondence to the hardware. There are no "extra" accesses with the PCI3IPmm design.

A long word access will automatically be converted into two back-to-back IP accesses with the address incrementing between cycles unless the increment disable function is selected (see control register description). For a read, one 32-bit data will be returned. For example a long word read to the ID space would yield 0xff50ff49 for many boards as the "0" location has $49 and the next address has $50. The long word mode happens automatically when all 4 of the byte lane enables are detected asserted. The overall throughput is greatly enhanced with this mode of operation.

The PCI3IPmm has a watchdog timer function, which completes the IP access if the IP does not respond within 7.6 us. The watchdog timer has a status bit and an optional interrupt output.

Each slot is programmable for 8 or 32 MHz. operation. The control register has separate bits for slot A, B, C and state-machine. The state machine speed defines the speed between cycles.

The PCI3IPmm supports interrupts from each slot with separate mask bits. Two interrupts from each of the three slots. In addition, an interrupt force bit is supplied to aid in software development. The masked interrupts are tied together and connected to INTA on the PCI bus.

The PCI3IPmm has LED's for power and user functions. The three voltages from slot A are connected to three LED's. An additional 6 LED's are supplied which are controlled via the control register for user-defined purposes.

An 8 bit "dip switch" is provided on the PCI3IPmm. The switch configuration is readable via a register. The switch is for user-defined purposes. We envision the switch being used for software configuration control or test purposes.

The reset switch provided can be used to reset the IP devices without affecting the PCI bus. Power-on, PCI reset, and the control register reset bit also cause the IP Reset to be activated. The reset is controlled to be synchronous to the 8 MHz clock. Alternatively, in development, the IP-Debug-Bus card also has a reset switch, which allows for individual slot resets.

The IO are brought to 50 pin headers.

The PCI3IPmm conforms to the VITA standard for IndustryPack Carriers. This guarantees compatibility with multiple IndustryPack compatible modules.

If your project can benefit from a "non-standard" implementation, or features that we have not thought of, or implemented yet please let us know. For example, if your project will use IP's that can operate at 33 MHz instead of 32, then we could synchronize the IP and PCI clocks and save several synchronization steps.

Theory of Operation

The PCI3IPmm is used to act as a bridge from PCI to IP bus specifications. The PCI bus will be the master in most cases with the IP boards being accessed for read or write cycles. The PCI accesses are handled at the lowest level by the PCI core.

The PCI bus provides multiplexed address and data plus control lines. The data is separated from the address and the control lines decoded to provide the inputs to the IP Interface state machines. The address is tested to determine which slot the access belongs to and which type of access. The IP strobes are generated. When acknowledge is detected to be asserted the cycle is terminated back to the host. The PCI bus will see a retry mode while the access is taking place and "disconnect with data" when the cycle is completed.

Feature List Current

• 3 IP compatible slots
• 8 or 32 MHz operation in each slot independently
• byte, word, long word access
• Incrementing or static access to each IP slot from long word access
• Bus error abort response
• 1:1 50 pin headers with .012" traces between IO and header
• IP Reset Switch
• 8 position "DIP Switch"
• 6 User LED's
• 3 Power LED's
• Fused Filtered Power with resettable fuses in each slot.
• Continued development with a "PROM" program

We plan to add several drivers for various products including the PCI3IPmm to our product line. If you develop a driver for one of our products and are willing to allow others to use it we will add it to the web site as a free of charge download and, if desired, give credit to the author.

As Dynamic Engineering adds features to the hardware we will update the PCI3IPmm page on the Dynamic Engineering website. If you want some of the new features, and have already purchased hardware, we will support you with a PROM update. We will ship a new PROM with the updated program to you for shipping plus $25 for the first PROM and $15 per device after that when ordered at the same time. If you are interested please send a PO with shipping instructions, the serial numbers of the boards to upgrade and the programming charge.

The basic PCI identifying information will not change with the updates. The revision field will allow configuration control. Current revision is 0x01.

Firmware Revision Table
A   Initial Release

Address Map

```
Function                      Offset      description

// PCI  relative addresses //
#define pci3ip_intreg_0        0x00000000  base cntl reg
#define pci3ip_intreg_1        0x00000004  interrupt request read back
#define pci3ip_intreg_2        0x00000008  read back of switch
// control register internal to Xilinx part. clock selection, interrupt
enable and set, IPACK size //

#define pci3ip_ida_st          0x00000200  start address slot A ID space
#define pci3ip_ioa_st          0x00000280  start address slot A IO space
#define pci3ip_inta_st         0x00000300  start address slot A INT space
#define pci3ip_mema_st         0x00000380  start address slot A MEM space
#define pci3ip_mema_en         0x000003ff  end address slot A MEM space

#define pci3ip_idb_st          0x00000400  start address slot B ID space
#define pci3ip_iob_st          0x00000480  start address slot B IO space
#define pci3ip_intb_st         0x00000500  start address slot B INT space
#define pci3ip_memb_st         0x00000580  start address slot B MEM space
#define pci3ip_memb_en         0x000005ff  end address slot B MEM space

#define pci3ip_idc_st          0x00000600  start address slot C ID space
#define pci3ip_ioc_st          0x00000680  start address slot C IO space
#define pci3ip_intc_st         0x00000700  start address slot C INT space
#define pci3ip_memc_st         0x00000780  start address slot C MEM space
#define pci3ip_memc_en         0x000007ff  end address slot C MEM space
```

FIGURE 1   PCI3IPMM ADDRESS MAP

The address map provided is for the local decoding performed within PCI3IPmm. The addresses are all offsets from a base address. The host that the PCI3IPmm is installed into provides the base address and interrupt level.

The host system will search the PCI bus to find the assets installed during power-on initialization. The VendorId = Ox1OEE and the CardId = OxOOOE for the PCI3IPmm. Interrupts are requested by the configuration space. PCIView and other third party utilities can be useful to see how your system is configured.

The VendorId and CardId parameters need to be set in the registry [NT]. The interrupt level expected and style is also set in the registry. Dynamic Engineering recommends WinRT to provide the low level hardware interface for Windows based systems.

Once the initialization process has occurred and the system has assigned an address range to the PCI3IPmm card, the software will need to determine what the address space is. We refer to this address as base0 in our software.

The next step is to initialize the PCI3IPmm. The main control register is written to for clock selection, and interrupt mask. The default of no interrupts enabled and 8 MHz operation will be valid in many cases.

Programming

The following is the initialization sequence that we use for our test software in an NT environment. We use a program called WinRT to do the low level accesses to the hardware. We use MS Visual C++ in conjunction with WinRT to write our test software. Please feel free to copy the following set-up code or to consider purchasing our engineering kit, which comes with our test suite.

```
#include "G_ALL.h"

unsigned long int base0, address, data, iWinRTlength;
unsigned long int data_in, data_s, data_out, errorCode, error;
unsigned long int reg, reg_copy, result, i, j;

long int pci3ip_init() {
  HANDLE hWinRT = WinRTOpenDevice(0, FALSE);
  WINRT_CONFIGURATION configBuf;
  DWORD iWinRTlength;
  if (WinRTGetConfiguration(hWinRT, &configBuf, &iWinRTlength) != 0)
  {
    base0 = configBuf.memMin;

Your Software Goes Here accesses are relative to base0
    WinRTCloseDevice(hWinRT);
    return(0);
    }
  else
    printf("Error: %d\n", GetLastError());
    WinRTCloseDevice(hWinRT);
    return(1);

 }
```

Register Definitions

pci3ip_intreg0

[$00 Main Control Register Port read/write]

<table>
<tr><td colspan="2" align="center">CONTROL REGISTER 0</td></tr>
<tr><td align="center">DATA BIT</td><td align="center">DESCRIPTION</td></tr>
<tr><td align="center">31</td><td>Reset 1 = reset IPs 0 = normal</td></tr>
<tr><td align="center">30</td><td>spare</td></tr>
<tr><td align="center">29</td><td>LED5 1 = ON 0 = OFF</td></tr>
<tr><td align="center">28</td><td>LED4</td></tr>
<tr><td align="center">27</td><td>LED3</td></tr>
<tr><td align="center">26</td><td>LED2</td></tr>
<tr><td align="center">25</td><td>LED1</td></tr>
<tr><td align="center">24</td><td>LED0</td></tr>
<tr><td align="center">23</td><td>spare</td></tr>
<tr><td align="center">22</td><td>spare</td></tr>
<tr><td align="center">21</td><td>Bus Error Int/Status Clear</td></tr>
<tr><td align="center">20</td><td>Bus Error Int En</td></tr>
<tr><td align="center">19</td><td>RES</td></tr>
<tr><td align="center">18</td><td>RES</td></tr>
<tr><td align="center">17</td><td>High Word Access C</td></tr>
<tr><td align="center">16</td><td>Increment Disable C</td></tr>
<tr><td align="center">15</td><td>High Word Access B</td></tr>
<tr><td align="center">14</td><td>Increment Disable B</td></tr>
<tr><td align="center">13</td><td>High Word Access A</td></tr>
<tr><td align="center">12</td><td>Increment Disable A</td></tr>
<tr><td align="center">11</td><td>INT FORCE 1 = FORCE 0 = NORMAL</td></tr>
<tr><td align="center">10</td><td>INT EN C1 1 = ENABLED 0 = DISABLED</td></tr>
<tr><td align="center">9</td><td>INT EN C0</td></tr>
<tr><td align="center">8</td><td>INT EN B1</td></tr>
<tr><td align="center">7</td><td>INT EN B0</td></tr>
<tr><td align="center">6</td><td>INT EN A1</td></tr>
<tr><td align="center">5</td><td>INT EN A0</td></tr>
<tr><td align="center">4</td><td>SPARE</td></tr>
<tr><td align="center">3</td><td>CLK SEL DEFAULT 1 = 32 0 = 8</td></tr>
<tr><td align="center">2</td><td>CLK SEL C</td></tr>
<tr><td align="center">1</td><td>CLK SEL B</td></tr>
<tr><td align="center">0</td><td>CLK SEL A</td></tr>
</table>

FIGURE 2   PCI3IPMM CONTROL PORT

Reset when set causes a reset to the IP slots. Reset is active as long as the Reset signal is asserted.

LED5-O are the user LED's situated just below the power status LED's near Slot A. Each LED can be activated by setting the corresponding data bit and deactivated by clearing the same bit.

Spare means unused and unplanned

RES means unused and planned for future enhancements

INT FORCE will when set cause INTA on the PCI bus to be asserted. This bit can be useful for software debugging. Set this to simulate an IP interrupt when the hardware is not available.

INT EN AO..C1 individual masks for the 2 interrupts from each of the three slots. O corresponds to INTO and 1 corresponds to INT1.

CLK SEL Default is set to cause the statemachine for the IP interface to operate at 32 MHz. when not accessing IP hardware. O sets the default speed to 8 MHz.

CLK SEL A,B,C are used to select the slot clock speed.
1 = 32 MHz. O = 8 MHz. PLL used to generate and low skew drivers to allow switching the clock speed on-the-fly.

Increment Disable A,B,C, when '1', turns off the address increment, for the respective slot, that normally occurs between 16-bit IP cycles when a 32-bit PCI access is performed. This is useful if, for instance, a FIFO is mapped to a single IP address since it allows double IP accesses to the same address with a single PCI transfer. All types of access are affected (i.e. MEM, IO, INT, and ID). Only 32 bit accesses are affected.

High Word Access A,B,C controls which 16-bit word is accessed when the Increment Disable is asserted. When 'O' the lower word is accessed twice, when '1' the upper word is accessed twice. This bit only has an effect when the Increment Disable bit is '1'. For correct functioning, make sure the PCI access is on a long-word boundary.

Bus Error Int En when '1' allows the bus error detection circuit to cause an interrupt to the host when a Bus Error is detected. The status is available on the Interrupt status register. When 'O' the status is still valid but no interrupt is generated when a bus error is detected. The bus error is detected when an access to one of the 3 IP slots is not responded to by IP hardware within the time-out period of approximately 7.6 us. The bus error circuit is always enabled and automatically responds as if the IP had responded. The data read will typically be $FF if the IP is not driving the bus for a bus error read. For a bus error write the write should be assumed to not have taken place. The host will not know that the bus error has taken place unless the host checks the status. The interrupt can provide a prompt to check the status during operation. During initialization if the

software is checking to "see" what is installed or what address range is valid on an IP then the status can be polled to see if the IP responded.

Bus Error Status/INT Clear when '1' will clear the status bit and interrupt request (if enabled). The Clear bit needs to be reset to 'O' to be able to capture the next Bus Error. The bus error timer hardware operates independent of clearing the status and will continue to monitor and intercede whether the status is read or cleared.

pci3ip_intreg1

[$04 pci3ip interrupt register read only]

CONTROL REGISTER 0	
DATA BIT	**DESCRIPTION**
31-15	unused
14	Bus Error 1= occurred 0 = none
13	UNMASKED C1
12	UNMASKED C0
11	UNMASKED B1
10	UNMASKED B0
9	UNMASKED A1
8	UNMASKED A0 1 = SET 0 = NOT SET
7	INTRN 1 = SET, 0 = NOT SET
6	INT FORCE
5	MASKED C1
4	MASKED C0
3	MASKED B1
2	MASKED B0
1	MASKED A1
0	MASKED A0 1 = SET 0 = NOT SET

FIGURE 3   PCI3IPMM INTERRUPT STATUS PORT

The interrupt requests from each of the IP slots are available as status from this port. The interrupt requests are inverted to make them active high for software usability. The requests are available in a masked and unmasked form to allow polling with the PCI interrupt masked off. When an interrupt is detected this register should be accessed to determine the source or sources and then appropriate action take to clear the interrupt at the IP or clear the mask on pci3ip_intregO.

The PCI3IPmm provides direct access to the interrupt space. If the IP causing the interrupt requires an interrupt vector fetch to clear the interrupt then the appropriate INT space should be accessed. Address bit A1 selects between IntO and Int1. A1 follows the word address to allow

access to both INTO and INT1 clearing addresses within the INT space.

If the IP does not require a Vector fetch then proceed with IO or other accesses as necessary.

The Bus Error status bit is set high when a Bus Error is handled by the internal watchdog timer circuit. The status will stay high until cleared with the Bus Error Int/Status Clear bit in the base control register. The Bus Error status bit is OR'd into the interrupt request logic and if enabled will cause a level sensitive interrupt to the host. The interrupt will remain asserted until the status is cleared.

pci3ip_intreg2

[$08 User Switch Port read only]

CONTROL REGISTER 0	
DATA BIT	DESCRIPTION
7..0	Sw7..0

FIGURE 4   PCI3IPMM USER SWITCH PORT

The user switch is read through this port. The bits are read as the lowest byte. Access the port as a long word and mask off the upper bytes. The switches are pulled-up on the board and the dipswitch when "on" grounds the corresponding bits. ("OFF" = 1 and "ON" = 0 in the PCI3IPmm silkscreen).

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID Ox1OEE and CardId OxOOOE and an interrupt level. Look quickly! If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView from Bsquare.
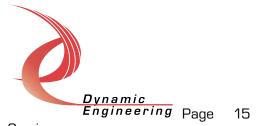
Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCI3IPmm when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the IP's installed into the PCI3IPmm than the PCI3IPmm itself, and it is smart system design when it can be achieved.

Connector definition. Slot A's IO connector is tied 1:1 to J5 which is nearest the card edge on the Slot A side. Slot B is tied to J4 and Slot C to J2.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The PCI3IPmm is constructed out of 0.062-inch thick FR4 material. We used .010 wide traces to add to the robustness of the interface design and .012+ for the connection between the IO connector

and headers. The trace widths and density of parts required a 6-layer board.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amps per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP Module can be secured against the carrier with the connectors. If more security against vibration is required then IP mounting kit can be used to attach the IP to the carrier.

Thermal Considerations

The PCI3IPmm design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air-cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

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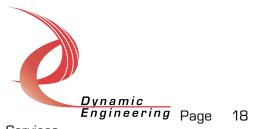
Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

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435 Park Dr.
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Specifications

Logic Interfaces:	IP Logic Interface, PCI Interface - 33 MHz, 32 bit
Access types:	IO, ID, MEM, INT IP Spaces supported via PCI bus accesses
CLK rates supported:	8 MHz or 32 MHz slot by slot selectable 33 MHz PCI
Software Interface:	Control Registers, and Installed IP
Initialization:	Programming procedure documented in this manual
Access Modes:	LW, Word or Byte to IP registers LW to Internal PCI Interface Control registers
Access Time:	Typical access time with 32 MHz. IP and double access mode is 500 ns.
Interrupt:	2 Interrupts per IP slot with separate enables.
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface:	50 pin Header Connectors
Dimensions:	1/2 length PCI board.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	2.17 W/^{O}C for uniform heat across IP
Power:	Filtered and fused to each IP slot. Resettable fuses. LED's (3) on slot A power ($\pm$12,5)
User	8 position software readable switch 6 software controllable LED's

Order Information

standard temperature range 0-70ºC
PCI3IPmm   1/2 length PCI card with 3 IP positions

extended temperature range -20 - 85ºC
PCI3IPmm-ET   1/2 length PCI card with 3 IP positions

PCI3IPmm-ENG   Engineering Kit for the PCI3IPmm
Software, Schematic, Debugging tools

IP-DEBUG-BUS   http://www.dyneng.com/ipdbgbus.html
IP test points, reset switch, fused power, quick
switch isolated interface lines to allow hot swapping
of IP cards.

IP-DEBUG-IO   http://www.dyneng.com/ipdbgio.html
Isolate the IO connector to help with debugging. 50
pin header for system cable connection. 50
testpoints suitable for wire-wrap to allow loop-back
connections. Locations for power and user circuits.

HDRterm50   http://www.dyneng.com/HDRterm50.html
50 pin header to 50 screw terminal converter with
DIN rail mounting.

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FIGURE 5   PCI3IPMM CONNECTOR REFERENCE

The PCI3IP has three slots (A,B,C) and three header connectors associated with those slots.

The wiring is 1:1 from the IP IO connector to the PCI3IP header connector. The connectors are numbered to match standard ribbon cable as shown in the figure to the right.

The IO connector traces are .012" in width.

Pin 50 Pin 49

Pin 2 Pin 1

50 Pin Header