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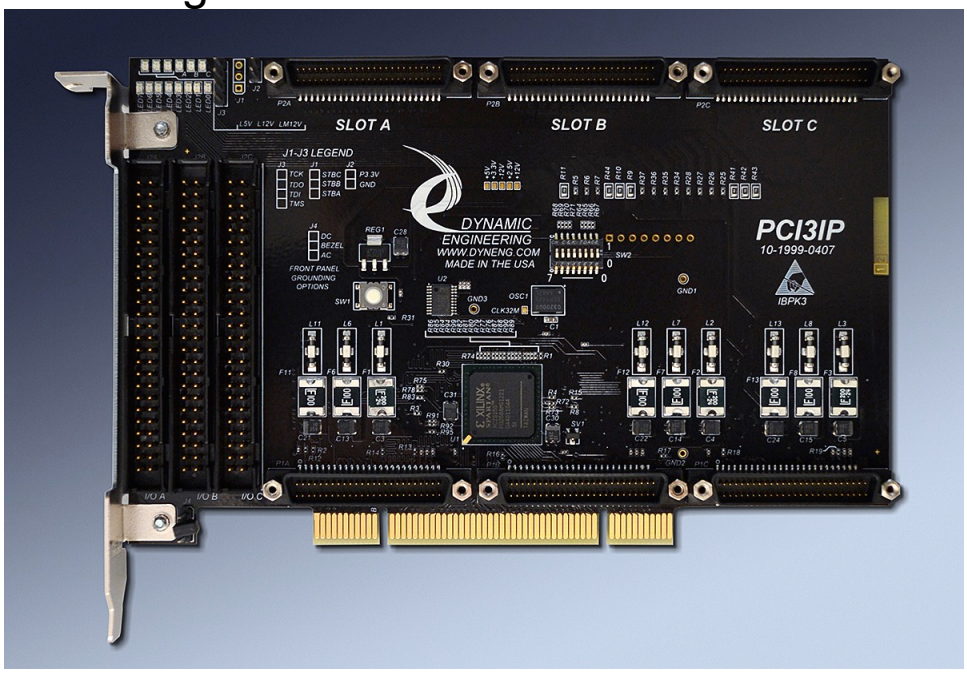
Est. 1988

PCI3IP

User Manual

Integrated PCI ⇔ IP Module Carrier



Key Features

Fast Access with integrated PCI ⇔ IP Bridge
3 IP Positions with IO
8/32 MHz IP operation 8/16/32 bit accesses supported
Data Alignment – Byte and Word Swapping
Watch Dog Timer
LEDs - Power, IP Access, User
Multi-board support

Manual Revision 07p3
Corresponding PCB: Revision 11
Fab Number: 10-1999-0411

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Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Modules and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised 3/15/21

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Product Description

IndustryPack® Modules are an important part of solutions for Embedded situations. Rugged, Small, light .. just right for many applications. IndustryPack® Modules require a “carrier” in most cases to adapt them to the system. Dynamic Engineering has carrier solutions for a variety of formats. The PCI3IP is designed to support PC computer based solutions. Other supported formats include PCIe, cPCI, PC104p, VPX.

Please note: PCIe3IP is a similar design with advanced features for the PCIexpress bus. PCIe3IP is also available with a separate Dynamic Data Sheet. http://www.dyneng.com/PCIe3IP.html

PCI3IP is part of the IP Compatible family of modular I/O components. PCI3IP provides three IndustryPack® module sites in one PCI slot.

PCI3IP is supported with Windows® compliant drivers for Win10 as well as Linux. The drivers come with a generic IP driver to allow use with “unknown” IP’s – IP’s that do not have a driver designed yet. For example, third party IPs.

The PCI accesses are handled by the PCI core. The IndustryPack® interface is controlled by the IP core. All of the logic is in VHDL making adaptations to user requirements reasonable to do.

Dynamic Engineering has made several updates to add new – user requested – features to this design and welcomes more new ideas for implementation. Dynamic Engineering makes every effort to keep backward software compatibility when new features are implemented. Set all unused bits to “0” when accessing to remain compatible with new features as they arise. “0” will correspond to the “old way” and “1” to enabling the new feature.

The PCI3IP design is flexible supporting each of the slot options with slot specific registers and independent operation.

ID, IO, INT, and MEM access types are supported for read and write cycles. The full 8 Mbytes of address space is allocated to each of the MEM spaces. A smaller memory footprint “mini map” version is available with a smaller MEM Space.

The PCI bus is 32 bits wide and most industry packs are 16 bit devices. Byte, word, and long word accesses are supported. Bytes can be to any address. Word accesses need to be word aligned. Long word accesses need to be long

word aligned. Each of the access types has a one-to-one correspondence to the hardware. There are no "extra" accesses with the PCI3IP design.

A long word access will automatically be converted into two back-to-back IP accesses with the address incrementing between cycles unless the increment disable function is selected (see control register description). For a read, one 32-bit data will be returned. For example a long word read to the ID space would yield 0xff50ff49 for many boards as the "0" location has $49 and the next address has $50. The long word mode happens automatically when all 4 of the byte lane enables are detected asserted. The overall throughput is greatly enhanced with this mode of operation.

A new addition to the design of the PCI3IP is to tag all accesses from the PCI bus. IP Modules can take longer than the PCI response specification leading to the use of retry cycles on the PCI bus. In a single CPU system the retry accesses are done serially. The current IP access will be the correct one to respond to the retry access. In a multi-CPU system it is possible to get out of sequence accesses, and potentially have the IP response sent to the wrong retry access. By storing the PCI parameters for the IP access and only responding to the correct retry cycle; multiprocessor cross contamination is avoided. This feature is new with the revision J and later program. Current revision PCB's have FLASH to store the Spartan II program and can be field updated.

PCI3IP has a watchdog timer function, which completes the IP access if the IP does not respond within 7.6 uS. The watchdog timer has a status bit and an optional interrupt output.

Each slot is programmable for 8 or 32 MHz. operation. The control register has separate bits for slot A, B, C and state-machine. The state machine speed defines the speed between cycles. It is recommended to use the 32 MHz speed when your IP Module supports the higher rate. Shorter PCI access cycle times result and less traffic on the PCI bus, plus higher rates of execution for the control program.

PCI3IP supports interrupts from each slot with separate mask bits. Two interrupts from each of the three slots. In addition, an interrupt force bit is supplied to aid in software development. The masked interrupts are tied together and connected to INTA on the PCI bus.

PCI3IP has LEDs for power and user functions. The three voltages from slot A are connected to three LEDs. An additional 6 LEDs are supplied which are controlled via the control register for user defined purposes.

An 8 bit "dip switch" is provided on the PCI3IP. The switch configuration is readable via a register. The switch is for user defined purposes. We envision the switch being used for software configuration control or test purposes. The Dynamic Engineering drivers support using the switch for IP Module identification.

The PCI Bus is enumerated at each power up cycle. The address range for a particular PCI3IP / IP Module combination can change when changes are made to the system. By using the switch on the PCI3IP the particular carrier can be identified if there are more than 1 in the system. Each IP is further identified by slot for positive identification. It can be important to “know” which external device you are reading or controlling.

The ID is stored as a number on the IP module in a register designed for this purpose or reusing a register without side affects. The IP driver when it starts up reads the information and has it available in system memory for application access. With a dedicated register the information will remain after application use. With a double use register the information will be overwritten by the application. In either case the information is available from the IP Module Driver.

For Windows systems the location of the register and offset for the bits is stored into the “INF” file for the carrier driver. IP Modules have updated INF files stored along with the IP Module driver to allow updating of the version that came with the carrier to handle situations where the IP Module was developed more recently than the Carrier driver.

Drivers can be developed for third party products and integrated into the auto detecting, marking and loading system. Alternatively the “generic” IP driver can be used to access third party IP Modules without a specific driver. The Generic IP Module driver is supplied with the Carrier driver.

The Win10 driver model has been updated to support the PCI and PCIe based carrier versions. This is important because IP Module drivers developed for the updated model will work for either carrier type [PCI or PCIe].

The reset switch provided can be used to reset the IP devices without affecting the PCI bus. Power-on, PCI reset, and the control register reset bit also cause the IP Reset to be activated. The reset is controlled to be synchronous to the 8 MHz. clock. Alternatively, in development, the IP-Debug-Bus card also has a reset switch, which allows for individual slot resets.

With revision **11** the FPGA has been upgraded to a Spartan 6. 3 new registers are added along with a new feature called **"VPWR"**. VPWR is the voltage on the "5V" connection to the IP modules and terminations. The default is 5V to match the IP standard. The Reserved 1 pin is monitored on each IP position and if any are grounded the voltage changes from 5V [open] to 3.3V [grounded]. The VPWR 5V LED is illuminated in open mode and VPWR 3.3V LED is illuminated for the RES1 = GND mode. This feature is being added to all Dynamic Engineering carriers as the transition to Spartan 6 is implemented. Please note: Previous revisions VPWR = 5V independent of RES1.

The benefit of VPWR: Most FPGA's operate with 3.3V and are not 5V tolerant. To operate on the IP bus level shifters are required on both ends. IP Modules targeting Dynamic Engineering carriers for installation can remove the level shifters and ground the RES1 pin. In addition most IO does not require 5V and can use 3.3V to eliminate a power supply on the IP Module.

The power to each of the IP slots is individually filtered and fused for VPWR and ±12. The fuses are rated at 2A on the VPWR rail and 1.1A on the ±12V rails. PCI3IP is designed to route maximum power to each slot in parallel. The power supply capabilities for your chassis may provide additional constraints. Each slot filter has a separate RF filter, bulk capacitor, "self healing" fuse, and bipass capacitors. A bipass capacitor is located at each of the power pins on the PCI3IP with the bulk capacitor near the filter pin for optimum noise rejection, voltage hold-up and local filtering. For power hungry IP's the fuses can be replaced with a strap to allow for more than the specified current.

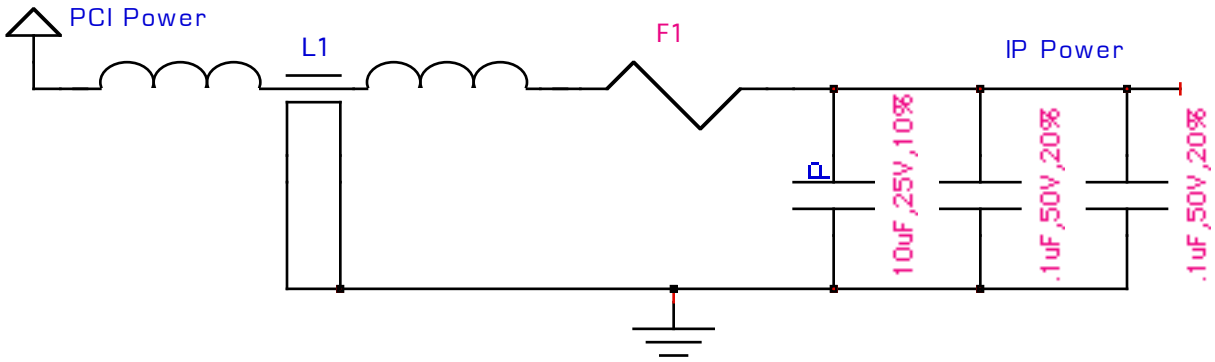


FIGURE 1 PCI3IP POWER FILTERING

With the filter pin on each slot and bulk capacitor each IP is effectively isolated from the other IP's mounted to the PCI3IP. Additional work was done in layout to

minimize the amount of cross-slot electronic noise. Each of the IP slots is also isolated from the PCI interface by the power conditioning. The FPGA uses 3.3, 2.5V, and 1.2V power which is derived from the 5V supply and bussed on mini-planes to the FPGA. The FPGA is effectively isolated from the IP slots by the regulators and additional filtering.

PCI3IP is well behaved with low noise power provided to each of the slots. PCI3IP is designed for analog and digital IP applications including data acquisition, instrumentation, measurement, command and control, telemetry and other industrial applications.

The IO are routed from the IP Module IO connector to individual 50 pin headers. The headers are suitable for ribbon cable or individual wire type connectors. HDRterm50 is a 50 in breakout connector that maps the 50 pin ribbon connector to 50 screw terminals for a neat, robust cabling system.
http://www.dyneng.com/HDRterm50.html

The IP position closest to the bezel has IO through the bezel with ejectors as the primary option. The Bezel is designed to support a right angle 50 position IDC header plus an arm to allow the cables from the other two positions to pass through the bezel. The default for the other two positions is no ejectors to retain PCI compliance for height on the component side of the card.

PCI3IP conforms to the VITA standard for IndustryPack Carriers. This guarantees compatibility with multiple IndustryPack compatible modules.

PCI3IP conforms to the PCI 2.3 specification and supports both 3.3V and 5V signaling levels. PCI3IP is accessible in the memory space on the PCI bus. This guarantees compatibility with other PCI compliant hardware – most PCs.

The PCI interface is integrated with the IP interface providing superior performance over designs relying on a separate PCI interface device. In addition to access speed the higher level of integration results in fewer initialization steps and requirements, more flexibility in operation, a higher MTBF, and less complex software with only one Base Address [BAR] to deal with.

Wired and User implemented. The IP Strobe signal is connected from each IP slot to a 3 pin header to allow for inter-slot user defined communications. The IP specification does not define what the strobe can be used for. The header is rarely used. If you need it please add “–STB” to your order number and we will install the 3 pin header for you. Standard .025” sq. posts suitable for wire-wrap inter-connection.

On each IP Slot the Strobe signal is connected to pin 46.

Theory of Operation

PCI3IP is used to act as a bridge from PCI to IP bus specifications. The PCI bus will be the master with the IPs accessed for read or write cycles.

The FPGA on the PCI3IP interfaces with the PCI interface and converts to the IP bus interface. The PCI bus provides multiplexed address and data plus control lines. The data is separated from the address and the control lines decoded to provide the inputs to the IP Interface state machines. The address is tested to determine which slot the access belongs to and which type of access. The IP strobes are generated. When acknowledge is detected asserted the cycle is terminated back to the host. The PCI bus will see a retry mode while the access is taking place and "disconnect with data" when the cycle is completed.

Each IP has 2 interrupts routed to the FPGA. Individual masks are used before combining to create the board level interrupt. Status is provided to determine the active interrupt sources.

The IP Module has Interrupt, ID, IO and Memory cycle types defined. The FPGA uses the stored cycle captured from the PCI bus to generate the appropriate cycle type to interact with the IP Module. The full IP Module Memory space is allocated for each IP module.

The PCI bus is 32 bits wide. The IP Module bus is 16 bits wide. Byte and word accesses are possible to the IP Modules on the PCI3IP. When LW accesses are attempted they are automatically broken into 2 accesses and both completed before acknowledging back to the PCI bus.

IP Modules can be operated at 8 or 32 MHz. Some IP Modules are restricted to 8 MHz only and some can do either frequency. It is recommended to use the highest frequency the IP Module is rated for. The PCI accesses will be shorter with the 32 MHz rate. Each slot on the PCI3IP is individually programmable to 8 or 32 MHz. 8 MHz is the default rate to allow all modules to operate in the default state.

Feature List

• PCI Universal Voltage [3.3 or 5V signaling]
• Integrated PCI ⇔ IP conversion for faster access
• 3 IP compatible slots
• Full ID, IO, INT, and Memory space allocated for each IP
• 8 or 32 MHz operation in each slot independently
• byte, word, long word access. 32 bit access to 16 bit slots with static or incrementing address. 32 bit access to 32 bit slots.
• byte and word swapping for little endian – big endian conversion
• Bus error abort response with slot status
• 1:1 50 pin headers with matched length, impedance controlled differentially routed traces between IO and header
• 8 position "DIP Switch"
• 8 User LED's
• 3 Power LED's
• Fused Filtered Power with “self healing” fuses in each slot.
• Continued development with FLASH updates available.
• SW option to use style slot register definitions or original PCI3IP design
• Slot-specific bus error latched status bit in the above slot registers
• Windows 10 drivers with IP Generic available for non DE IPs
• Linux driver with IP Generic available for non DE IPs.

We are adding new drivers for various products to our product line. All of the IP drivers added will work with any of our carrier designs. If you develop a driver for one of our products or a third party IP to work with our carrier and are willing to allow others to use it we will add it to the web site as a free of charge download and, if desired, give credit to the author.

The basic PCI identifying information will not change with the updates. The revision field will to allow configuration control.

Firmware Revision Table

A Initial Release
B Alter timing to accommodate non-compliant IP modules.
C Add 32 bit access feature
D Add bus error timer feature
E Update 32 bit access to allow static and auto-incremented address behavior
F Add separated registers for slots A,B,C and retain default of unified control register
G Add slot-specific bus error latched status in the separated registers. Add a force interrupt bit and IP interrupt status bits in the slot control register. Also change PCI class code to PCI bridge - subclass other.
H, I developmental control
J Multiprocessor capability added
K Recompiled into Spartan II
12p5 Updated for Win10 and compatiblilty with other carriers – added 3 registers.
13p0 Updated for Spartan VI implementation.

Address Map

Function	Offset	description
// PCI relative addresses //		
#define pci3ip_intreg_0	0x00000000	base cntl reg
#define pci3ip_intreg_Scr0	0x00000014 // new with 12p5 spare register	
#define pci3ip_intreg_Scr1	0x00000018 // new with 12p5 spare register	
#define pci3ip_intreg_DsgnInfo	0x0000001C // new with 12p5 – Type of Carrier	
#define pci3ip_intreg_1	0x00001000	interrupt request read back
#define pci3ip_intreg_2	0x00002000	read back of switch
#define pci3ip_alt_reg_A	0x00003000	Alternate control reg Slot A
#define pci3ip_alt_reg_B	0x00004000	Alternate control reg Slot B
#define pci3ip_alt_reg_C	0x00005000	Alternate control reg Slot C
// control register internal to Xilinx part. clock selection, interrupt enable and set, IPACK size //		
#define pci3ip_ida_st	0x50000	start address slot A ID space
#define pci3ip_idb_st	0x60000	start address slot B ID space
#define pci3ip_idc_st	0x70000	start address slot C ID space
#define pci3ip_ioa_st	0x90000	start address slot A IO space
#define pci3ip_iob_st	0xa0000	start address slot B IO space
#define pci3ip_ioc_st	0xb0000	start address slot C IO space
#define pci3ip_inta_st	0xd0000	start address slot A INT space
#define pci3ip_intb_st	0xe0000	start address slot B INT space
#define pci3ip_intc_st	0xf0000	start address slot C INT space
#define pci3ip_mema_st	0x00800000	start address slot A MEM space
#define pci3ip_mema_en	0x00ffffff	end address slot A MEM space
#define pci3ip_memb_st	0x01000000	start address slot B MEM space
#define pci3ip_memb_en	0x017fffff	end address slot B MEM space
#define pci3ip_memc_st	0x01800000	start address slot C MEM space
#define pci3ip_memc_en	0x01ffffff	end address slot C MEM space

FIGURE 2 PCI3IP ADDRESS MAP

The address map provided is for the local decoding performed within PCI3IP. The addresses are all offsets from a base address, which, along with the interrupt level, is provided by the host in which the PCI3IP is installed.

The host system will search the PCI bus to find the assets installed during power-on initialization. The VendorId = 0x10EE and the CardId = 0x0003 for the PCI3IP. Interrupts are requested by the configuration space.

Once the initialization process has occurred and the system has assigned an address range to the PCI3IP card, the software will need to determine what the address space is. We refer to this address as the base address. The Base Control register is located at this address and all others are offsets relative to this address. The first time through it is handy to use a PCI viewing tool to see the address space and interrupt assigned to the PCI3IP. The revision of the PROM is also shown with most tools.

The next step is to initialize the PCI3IP. The main control register is written to for clock selection, and interrupt mask. The default of no interrupts enabled and 8 MHz. operation will be valid in many cases.

For new software development it is recommended to use the channel control registers. The originial base control register is provided for legacy support.

Programming

Dynamic Engineering recommends using the PCI3IP Windows® or Linux drivers. The drivers will handle the system resources and provide a stable platform for your IP driver to work with. The Parent/Child driver combination is designed to provide plug-n-play operation with automatic loading of the required drivers and automatic selection of the generic driver if a matching IP driver is not found.

Each Dynamic Engineering Carrier has a unique “parent” driver to support it. Each of the drivers have been carefully designed to provide a consistent interface to the IP drivers. The consistency makes the IP driver completely portable between different carriers and different architectures. For example you can develop in your desktop PC and then port to your cPCI system without having to redo the IP driver.

Should you need to support a different OS or just want to do your own please refer to the memory map and register map information. All of the details needed to program the card are covered in those sections. Please feel free to send any questions to engineering@dyneng.com.

Register Definitions

pci3ip_intreg0

[$00 Main Control Register Port read/write]

CONTROL REGISTER 0

DATA BIT	DESCRIPTION
31	Reset 1 = reset IP's 0 = normal
30	spare
29	LED5 1 = ON 0 = OFF
28	LED4
27	LED3
26	LED2
25	LED1
24	LED0
23	LED7
22	LED6
21	Bus Error Int/Status Clear
20	Bus Error Int En
19	Alternate Register set selection
18	RES
17	High Word Access C
16	Increment Disable C
15	High Word Access B
14	Increment Disable B
13	High Word Access A
12	Increment Disable A
11	INT FORCE 1 = FORCE 0 = NORMAL
10	INT EN C1 1 = ENABLED 0 = DISABLED
9	INT EN C0
8	INT EN B1
7	INT EN B0
6	INT EN A1
5	INT EN A0
4	SPARE
3	Spare
2	CLK SEL C
1	CLK SEL B
0	CLK SEL A

FIGURE 3 PCI3IP CONTROL PORT

Reset when set causes a reset to the IP slots. Reset is active as long as the Reset signal is asserted.

LED5-0,7-6 are the user LEDs situated just below the power status LEDs near

Slot A. Each LED can be activated by setting the corresponding data bit and deactivated by clearing the same bit. Bits 6 and 7 were added with revision 5 fabs and are on previously spare bits to remain compatible with previous releases.

Spare means unused and unplanned

RES means unused and planned for future enhancements

INT FORCE will when set cause INTA on the PCI bus to be asserted. This bit can be useful for software debugging. Set this to simulate an IP interrupt when the hardware is not available.

Bus Error Int En when '1' allows the bus error detection circuit to cause an interrupt to the host when a Bus Error is detected. The status is available on the Interrupt status register. When '0' the status is still valid but no interrupt is generated when a bus error is detected. The bus error is detected when an access to one of the 3 IP slots is not responded to by IP hardware within the time-out period of approximately 7.3 uS. The bus error circuit is always enabled and automatically responds as if the IP had responded. For a bus error write the write should be assumed to not have taken place. The host will not know that the bus error has taken place unless the host checks the status. The interrupt can provide a prompt to check the status during operation. During initialization if the software is checking to "see" what is installed or what address range is valid on an IP then the status can be polled to see if the IP responded.

Bus Error Status / INT Clear when '1' will clear the status bit and interrupt request [if enabled]. The Clear bit needs to be reset to '0' to be able to capture the next Bus Error. The bus error timer hardware operates independent of clearing the status and will continue to monitor and intercede whether the status is read or cleared.

Please note that the Alternate Register Selection bit affects the following bit definitions. When '0' the base register definitions are used. When '1' the separated register definitions are used. For commonality with all other Dynamic Engineering Slot Control it is highly recommended to use the Alternate Control Registers for these bits. Bits remain to support the original clients.

CLK SEL A,B,C are used to select the slot clock speed.
1 = 32 MHz. 0 = 8 MHz. PLL used to generate and low skew drivers to allow switching the clock speed on-the-fly.

Increment Disable A, B, C, when ‘1’, turns off the address increment, for the respective slot, that normally occurs between 16-bit IP cycles when a 32-bit PCI access is performed. This is useful if, for instance, a FIFO is mapped to a single IP address since it allows double IP accesses to the same address with a single PCI transfer. All types of access are affected (i.e. MEM, IO, INT, and ID). Only 32 bit accesses are affected.

High Word Access A,B,C controls which 16-bit word is accessed when the Increment Disable is asserted. When ‘0’ the lower word is accessed twice, when ‘1’ the upper word is accessed twice. This bit only has an effect when the Increment Disable bit is ‘1’. For correct functioning, make sure the PCI access is on a long-word boundary.

INT EN A0..C1 individual masks for the 2 interrupts from each of the three slots. 0 corresponds to INT0 and 1 corresponds to INT1.

Pci3ip_intreg_Scr0

[$0014 Scratch Register read/write]

SCRATCH REGISTER 0	
DATA BIT	**DESCRIPTION**
31-0	Spare

FIGURE 4 PCI3IP SCRATCH REG 0

Pci3ip_intreg_Scr1

[$0018 Scratch Register read/write]

SCRATCH REGISTER 1	
DATA BIT	**DESCRIPTION**
31-0	Spare

FIGURE 5 PCI3IP SCRATCH REG 1

Two spare registers are provided. The registers are used as part of the test package to show the PCI bus is operational. The registers can be used for BIT should your system need that ability.

Pci3ip_intreg_DsgnInfo

[$001C Design Info read only]

Design Information	
DATA BIT	**DESCRIPTION**
31-24	Spare
23-20	Type
19-16	NumOfSlots
15-8	Reserved [CPLD not present]
7-4	Major Flash Revision
3-0	Minor Flash Revision

FIGURE 6 PCI3IP DESIGN INFO

The Design Information Register is added with revision 12p5 Flash to become compatible with the PCIeNIP carrier type and number of positions definitions. The Win10 combined driver reads this register and determines the type of carrier and if needed the number of positions. In addition certain status information is available.

Type Table:
x1 PCI3IP – value returned for this design
x2 PCI5IP
x3 cPCI2IP
x4 cPCI4IP
x5 PC104pIP
x6 PC104p4IP

NumOfSlots = x3 for this design.

Revision Fields are actually 8 bits each. Lower nibble of each is reported in this register. Full size values are available in the Switch register.

pci3ip_intreg1

[$1000 pci3ip interrupt register read only]

CONTROL REGISTER 1	
DATA BIT	**DESCRIPTION**
31-27	unused
26	Bus Error Slot C
25	Bus Error Slot B
24	Bus Error Slot A
23-15	unused
14	Bus Error 1= occurred 0 = none
13	UNMASKED C1
12	UNMASKED C0
11	UNMASKED B1
10	UNMASKED B0
9	UNMASKED A1
8	UNMASKED A0 1 = SET 0 = NOT SET
7	INTRN 1 = SET, 0 = NOT SET
6	INT FORCE
5	MASKED C1
4	MASKED C0
3	MASKED B1
2	MASKED B0
1	MASKED A1
0	MASKED A0 1 = SET 0 = NOT SET

FIGURE 7 PCI3IP INTERRUPT STATUS PORT

The interrupt requests from each of the IP slots are available as status from this port. The interrupt requests are inverted to make them active high for software usability. The requests are available in a masked and unmasked form to allow polling with the PCI interrupt masked off. When an interrupt is detected this register should be accessed to determine the source or sources and then appropriate action take to clear the interrupt at the IP or clear the mask on pci3ip_intreg0.

PCI3IP provides direct access to the interrupt space. If the IP causing the interrupt requires an interrupt vector fetch to clear the interrupt then the appropriate INT space should be accessed. Address bit A1 selects between Int0 and Int1. If the IP does not require a Vector fetch then proceed with IO or other accesses as necessary.

The Bus Error status bit is set high when a Bus Error is handled by the internal watch dog timer circuit. The status will stay high until cleared with the Bus Error

Int / Status Clear bit in the base control register. The Bus Error status bit is or'd into the interrupt request logic and if enabled will cause a level sensitive interrupt to the host. The interrupt will remain asserted until the status is cleared.

The seperated status for Bus Errors is also available to provide the slot information associated with the bus error. The status is also available in the individual control ports. All Bus Error bits are cleared together via the base register.

pci3ip_intreg2

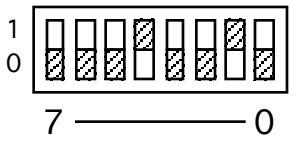
[$2000 User Switch Port read only]

CONTROL REGISTER 2

DATA BIT	DESCRIPTION
23-16	Revision Minor
15-8	Revision Major
7..0	Sw7..0

FIGURE 8 PCI3IP USER SWITCH PORT

The user switch is read through this port. The bits are read as the lowest byte. Access the port as a long word and mask off the undefined bits. Read only. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



The switch can be used for any user purpose or to identify a particular PCI3IP in a system with more than one card installed. Dynamic Engineering Driver software can use the switch for slot identification.

Revision.Major "p" Revision.Minor are read from this port as well. The revisions reflect the FLASH revision in use currently. See the earlier table. If all 0x00 except switch this feature is not implemented [earlier versions].

pci3ip_alt_regA-C

[$3000, 0x4000, 0x5000 Alternate Control Register bit defintions]

CONTROL REGISTER A,B,C	
DATA BIT	**DESCRIPTION**
17	Interrupt Status 1
16	Interrupt Status 0
15-9	Spare
8	Bus Error Status/Clear
7	Word Swap
6	Byte Swap
5	Interrupt Enable 1
4	Interrupt Enable 0
3	High Word Access
2	Increment Disable
1	Force Interrupt
0	Speed Control

FIGURE 9 PCI3IP ALTERNATE CONTROL REGISTER PORTS

Please note that the Alternate Register Selection bit affects the following bit definitions. When ‘0’ the base register definitions are used. When ‘1’ the following register definitions are used.

Speed Control selects the slot clock speed. 1 = 32 MHz. 0 = 8 MHz. Clock selection change can be made at any time. Each slot has a separate speed control bit. Default is 8 MHz.

Force Interrupt when ‘1’ causes an interrupt cycle, which will be interpreted as a IP slot interrupt. This bit was added to support interrupt service routine development when using the generic IP driver.

Increment Disable when ‘1’, turns off the address increment, for the respective slot; normally occurs between 16-bit IP cycles when a 32-bit PCI access is performed. This is useful if, for instance, a FIFO is mapped to a single IP address since it allows double IP accesses to the same address with a single PCI transfer. 32 bit accesses of all types of access are affected (i.e. MEM, IO, INT, and ID). 16 bit accesses are not affected.

High Word Access controls which 16-bit word is accessed when the Increment Disable is asserted. When ‘0’ the lower word is accessed twice, when ‘1’ the

upper word is accessed twice. This bit only has an effect when the Increment Disable bit is ‘1’. For correct functioning, make sure the PCI access is on a long-word boundary.

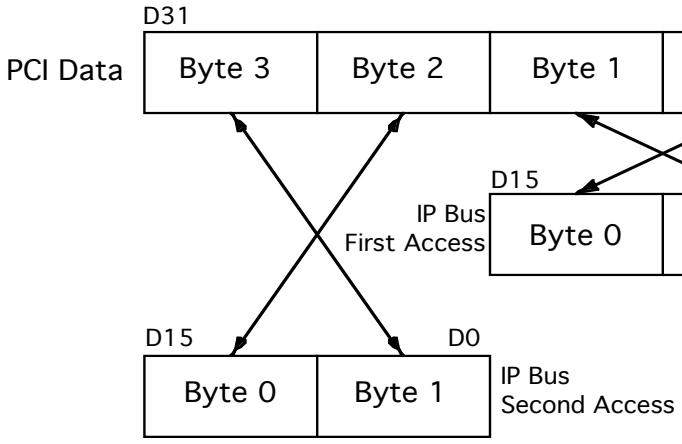
Interrupt Enable 0, 1: Individual masks for the two interrupts from the respective IP slot. 0 corresponds to INT0 and 1 corresponds to INT1. When these bits are ‘1’, the interrupt is enabled, when ‘0’ the corresponding interrupt is disabled.

The **bus erro**r bit is a status bit with a write clear. The clear is active at the time of the write only and does not need to be reset. If the bus error bit is set when the register is read then a bus error has occurred on this slot. Once set the bit will remain set until explicitly cleared by writing a ‘1’ to this bit position.

Interrupt Status 0, 1: These are read-only status bits indicating, when the bit is a ‘1’, that the corresponding IP interrupt is active. However, the interrupt will not be passed on to the PCI bus unless the respective interrupt enable is also set. *See also the Interrupt Status register which provides all positions in one read.*

Byte Swap when ‘1’ causes the byte lanes to be swapped. For a 16-bit access the upper byte is swapped with the lower byte. For a 32-bit access to a 16-bit port the upper and lower of each word are swapped. For a 32-bit access to a 32-bit port the bytes and words are swapped so D31-24 becomes D7-0 etc. Byte Swap when ‘0’ provides the data on the same byte lanes that the PCI bus provides them on. Byte Swapping can be used in conjunction with the Word Swap feature for big endian ⇔ little endian conversion.

16 bit ports



D15-8 ⇔ D7-0, D31-24 ⇔D23-16

FIGURE 10 PCI3IP BYTE SWAPPING

Word Swap when ‘1’ will cause the upper and lower words to be swapped. Data written to PCI D15-0 will be driven onto the IP bus as if it originated on D31-16. Word Swap when ‘0’ leaves the data on the PCI word definitions.

The IP bus interface state-machine will move data from D15-0 to the “0” address and from PCI D31-16 to the IP “2” address. IP addresses are word. The PCI bus will write data to either the upper or lower words and apply the corresponding CBE byte lane strobes. The PCI3IP hardware will translate the data to D15-0 on the IP.

Word swapping can be used effectively for big endian ⇔ little endian translation and to accommodate IP’s with registers that can be more effectively accessed in reverse order. For example: if the IP registers are organized with the MS data at address 0x00 and the LS data at 0x02 then a single 32 bit write can be made to 0x00 with address incrementing enabled and word swapping enabled so that the PCI D31-16 data is written to IP 0x00 and the PCI D15-0 data is written to IP 0x02. If the IP registers have data 16 bits or less then word swapping will not be needed.

With the combination of Byte and Word Swapping plus address definition any byte/word can be direct to/from any destination. Big ⇔ little endian issues can be resolved and IP architecture optimized for software access.

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID 0x10EE and CardId 0x0003 and an interrupt level. Look quickly! If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCI3IP when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the IPs installed into the PCI3IP than the PCI3IP itself, and it is smart system design when it can be achieved.

Connector definition. Slot A's IO connector is routed 1:1 to J5 which is nearest the card edge on the Slot A side. Slot B is tied to J4 and Slot C to J2. Please refer to the diagram near the end of the manual. The interconnection traces are differentially routed, impedance controlled, and matched length for each slot separately.

Cable egress bezel. A special bezel has been developed for the Dynamic Engineering IP Carrier series for PCI and PCIe. The IP Module IO connector closet to the bezel is right angle with ejectors providing direct access through the bezel.

The bezel has a hinged edge allowing the remaining cables to be installed with the “arm up” and then the arm fastened. This feature was developed to make true single slot operation practical. With cabling through the bezel on the same slot as the PCI5IP the adjacent slot can be utilized.

If the IO is to be used internal to the chassis the -BB option will remove the bezel and replace with the traditional blank model plus change the connector to a vertical one like the other positions.

Standard ribbon cable can be used as well as discrete wiring to the header connector. HDEterm50 provides a ribbon cable to screw terminal interface. Custom cables are available for specific IP Modules. See ordering information at the end of this document.

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the PCI3IP slots. Also see the User Manual for your IP board(s) for more information.

GND	GND	1	26
CLK	VPWR	2	27
Reset*	R/W*	3	28
D0	IDSEL*	4	29
D1	DMA-reserved	5	30
D2	MEMSEL*	6	31
D3	DMA-reserved	7	32
D4	INTSEL*	8	33
D5	DMA-reserved	9	34
D6	IOSEL*	10	35
D7	VPWR_SEL	11	36
D8	A1	12	37
D9	DMA-reserved	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTREG0*	17	42
D14	A4	18	43
D15	INTREQ1*	19	44
BS0*	A5	20	45
BS1*	Strobe	21	46
–12V	A6	22	47
+12V	Ack*	23	48
VPWR	RSVD	24	49
GND	GND	25	50

NOTE 1: The error signal is defined by the IP Module Logic Interface Specification, but not used by this Carrier. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. This table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the carrier.

Note 3: VPWR = 5V by default and can be selected to 3.3V by grounding VPWR_SEL on the IP Module.

FIGURE 11 PCI3IP LOGIC INTERFACE

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. Relatively small with two connectors and 4 added attachment points per IP Module. The carrier / adapter should match this construction to provide a complete package.

PCI3IP is constructed out of 0.062 inch thick High temp ROHS compliant FR4 material. Gold plated for corrosion resistance, superior thermal properties, and mechancial strength (solder adhession). Both ROHS and standard processing are available. Standard is the default and is the traditional leaded solder method. ROHS uses ROHS compliant devices and solder/flux etc.

All units are fully tested with IP-Test running our Win10 based test suite. This loads the power supplies and provides a good stress test of the units. IP-Test is a special FLASH load for IP-Parallel-HV with ID, IO, INT, MEM cycle support plus both interrupts, the ability to create Bus Errors etc.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amps per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP Module can be secured against the carrier with the connectors. If more security against vibration is required then IP mounting kit can be used to attach the IP to the carrier.

Thermal Considerations

PCI3IP design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. Components are rated for -40 ⇔ +85C. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished. The installed IP Modules will be the driving factor in thermal calculations.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
support@dyneng.com

Specifications

Logic Interfaces:	IP Logic Interface, PCI Interface -33 MHz. 32 bit Universal Voltage
Access types:	IO, ID, MEM, INT IP Spaces supported via PCI bus accesses
CLK rates supported:	8 mhz or 32 MHz slot by slot selectable 33 MHz. PCI
Software Interface:	Control Registers, and Installed IP
Initialization:	Programming procedure documented in this manual. Default to 8 MHz, interrupts disabled.
Access Modes:	LW, Word or Byte to IP registers LW to Internal PCI Interface Control registers
Access Time:	Depends on IP Module installed. State-Machine controlled, PCI compliant.
Interrupt:	2 Interrupts per IP slot with separate enables.
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface:	50 pin Header Connectors
Dimensions:	1/2 length PCI board.
Construction:	High Temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across IP
Power:	Filtered and fused to each IP slot. Resettable fuses. LEDs (3) on slot A power (±12,5)
User	8 position software readable switch 8 software controllable LEDs
Components	Industrial Temp rated or better.

Order Information

Standard temperature range -40⇔85C

PCI3IP	1/2 length PCI card with 3 IP positions. Egress bezel, right angle header with ejectors for position A, standard solder. https://www.dyneng.com/pci_3_ip.html
-BB	Front Panel without egress to facilitate cabling to the outside through the PCI3IP Bezel "Blank Bezel" Vertical connector installed for position A.
-ROHS	Use ROHS processing. Please note: standard "leaded" solder etc. used without this option. Boards with ROHS processing are marked "ROHS".
-EJ	Use Header Connectors with ejectors installed. Please note the increased height will be taller than PCI specification – for end slots or with an open slot next to the PCI3IP
IP-DEBUG-BUS	https://www.dyneng.com/ipdbgbus.html IP test points, reset switch, fused power, quick switch isolated interface lines to allow hot swapping of IP cards.
IP-DEBUG-IO	https://www.dyneng.com/ipdbgio.html Isolate the IO connector to help with debugging. 50-pin header for system cable connection 50 testpoints suitable for wire-wrap to allow loop-back connections Locations for power and user circuits
HDRterm50	https://www.dyneng.com/HDRterm50.html 50-pin header to 50-screw terminal converter with DIN rail mounting
HDRribn50	https://www.dyneng.com/HDRribn50.html Ribbon cable with strain relief and cable pull tab Available in custom lengths. Standard and Twisted pair.

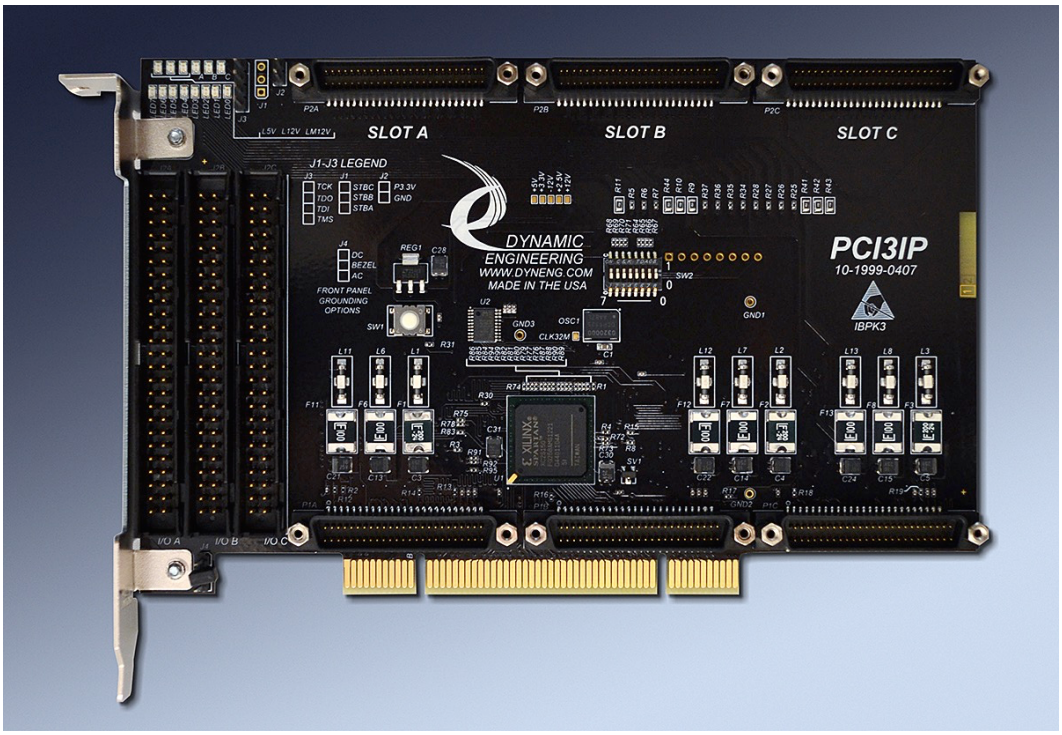
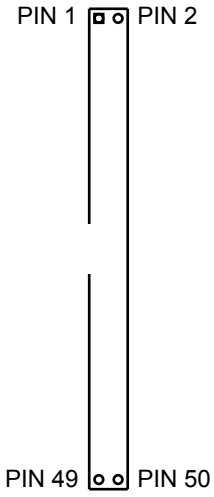


FIGURE 12 PCI3IP CONNECTOR REFERENCE



PCI3IP has three slots (A,B,C) and three header connectors associated with those slots.

The traces are connected 1:1, differentially routed, matched length, impedance controlled from the IP IO connector to the PCI3IP header connector. The Box Headers are numbered to match standard ribbon cable as shown in the figure to the left.

Rev 07 shown. Current models have the cable egress bezel with a right angle header for position A.