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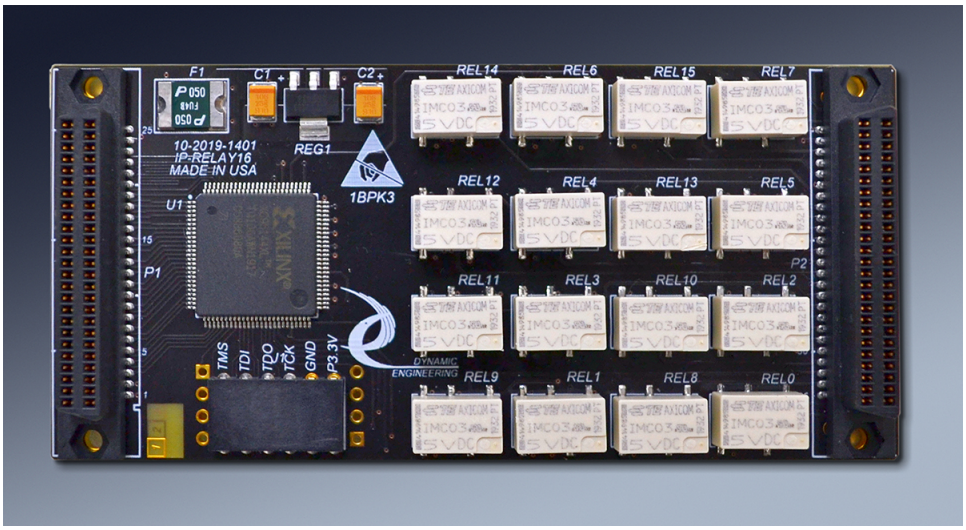
Est. 1988

User Manual

IP-Relay16

16 Form C (SPDT) Relays
IP Module



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IP-Relay16
16 Form C Relays
IP Module

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Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised 03/18/20

Table of Contents

List of Figures

Product Description

IP-Relay16 is part of the IP Module family of modular I/O components. IP-Relay16 is designed to provide 16 SPDT [FORM C] relays suitable for Normally Open “NO” and Normally Closed “NC” applications. The Relays are rated for 220VDC, 250VAC, switching current = 4A, 3A continuous. The traces on IP-Relay16 are designed to handle 1.5A+. The IP connectors will limit to 1A continuous.

An Industrial Temperature Xilinx CPLD device is used to implement the IP interface and provide the control register for the Relays. SW can enable or disable each relay independently. All three of the NO, NC, COM connections are available at the IP IO connector.

The controlling register resets to 0x0000 putting the relays into their default state of the NO side open and the NC side closed referenced to the COM.

IP-Relay16 supports 8 and 32 MHz IP Bus operation.

The IDPROM is implemented to allow identificatoin of the device. In addition a Revision register is available to read the FLASH version installed.

The Xilinx has room for additional features or custom protocols. Please see our web page for current protocols offered. If you do not find it there we can redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please contact Dynamic Engineering with your custom application.

The relays use 5V to energize, and the CPLD is a 3.3V device. Transistors are controlled by the Relay Control register. When the transistor(s) are enabled the ground for the relay is connected via the transistor to complete the circuit and enable the Relay to switch states. See Figure 1. Discrete components are used for superior thermal properties, to reduce single point failure paths, and to allow optimal placement of the Relay - transistor circuits. Back EMF protection is provided.

All configuration registers support read and write operations for maximum software convenience. Word operations are supported (please refer to the memory map).

IP-Relay16 conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Since the IP maintains plug and software compatibility while mounted on different form factors, system prototyping may be done on one IP Carrier board, with final system implementation done on a different one.

Theory of Operation

IP-Relay16 features a Xilinx CPLD. The CPLD contains all of the registers and protocol controlling elements of the IP-Relay16 design. Only the Relays and related circuitry are external to the Xilinx.

IP-Relay16 is a part of the IP Module family of modular I/O products. It meets the IP Module Vita Standard. In standard configuration it is a Type II mechanical with low profile components on the back of the board and one slot wide. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

A logic block within the Xilinx device contains the decoding and timing elements required for the host CPU to interface via the IP bus. The timing is referenced to the 8 or 32 MHz IP logic clock. The IP responds to the ID, INT, MEM, and IO selects. IP-Relay16 design requires one wait states for read or write cycles to any IO address. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host removes the SEL line. Local timing terminates a write cycle prior to the SEL being de-asserted.

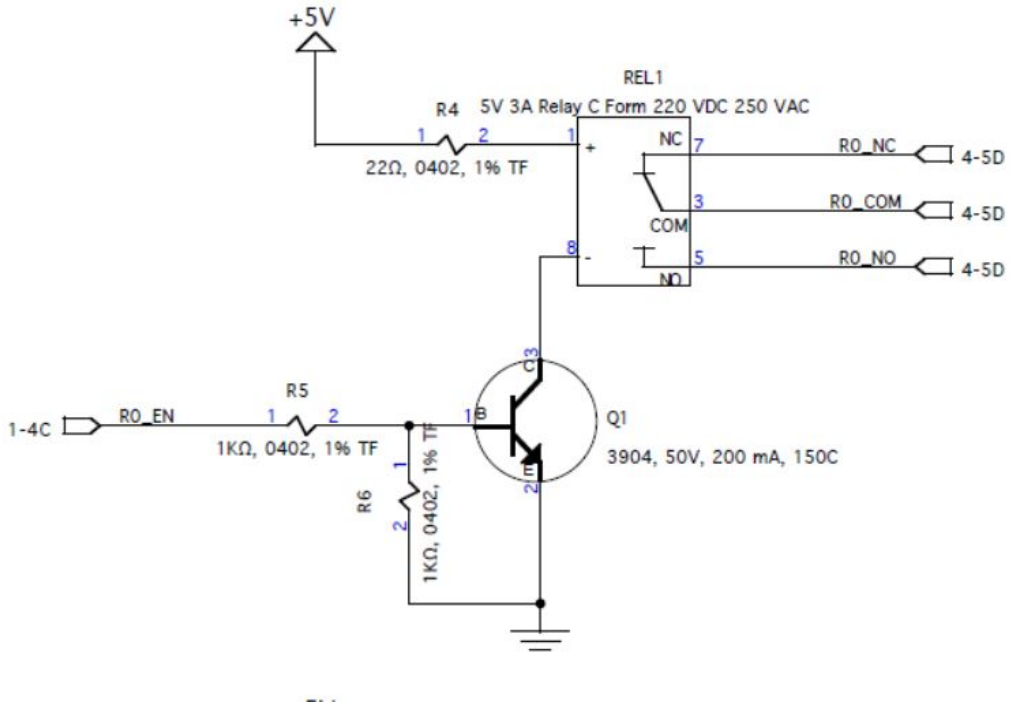

FIGURE 1 IP-RELAY16 DIAGRAM

Please remember the IP can switch the controls faster than the output can change states. If IP-Relay16 is commanded to change the state of an output at a rate faster than the transition time for your system partial switching will result.

Additional Relay Details.

- UL rated.
- RoHS/ELV, China RohS, REACH compliant.
- IEC 61810 RT V – hermetically sealed [category of environmental protection]
- IEC 60529 IP 67, immersion cleanable [degree of protection]
- 10^8 operations rated per relay. Contact life depends on power transfer.
  - 30W ~ 500,000 operations
  - 60W ~ 100,000 operations
  - low wattage ~ 2,000,000 operations
- 60W, 62.5 VA rated switching power. For example 30V and 2A. 4A max.
- 220VDC/250VAC
- Relays incorporate bifurcated contacts, and support high mechanical shock.
  - Vibration resistance (functional) 20g, 10 to 500 Hz
  - Shock resistance (functional), half sinus 11 mS 50g
  - Shock resistance (destructive), half sinus .5 mS 500g
- PdRu twin contacts, Gold covered.
- 1mS operate time typical. 3 mS max.
- Release time without diode in parallel typ = 1 mS, max = 3 mS.
- Release time with diode in parallel 3 mS typical, 5 mS max.
- Bounce time 1 mS typical, 5 mS max.
- Cross Talk 100 MHz/900 MHz ⇔ -37dB/-18.8 dB
- Insertion loss 100 MHz/900 MHz ⇔ 0.03dB/0.33dB
- VSWR [Voltage Standing Wave Ratio] 100 MHz/ 900 Mhz ⇔ 1.06/1.49
- Initial Dielectric Strength:
  - between open contacts ⇔ 1000 Vrms
  - between contact and coil ⇔ 1800 Vrms
- Initial surge withstand voltage
  - between open contacts ⇔ 1500 V
  - between contact and coil ⇔ 2500 V
- Capacitance:
  - max 1pF between open contacts
  - max 2pF between contact and coil

Address Map

Function	Offset	Type
Relay Control	0x00000000	0 base control address
	0x00000002	1 unused
	0x00000004	2 unused
	0x00000006	3 unused
Relay Revision	0x00000008	4 Major and Minor Revision Read only
	0x0000000a	5 unused
	0x0000000c	6 unused
	0x0000000e	7 unused

FIGURE 2 IP-RELAY16 INTERNAL ADDRESS MAP

The address map provided is for the local IO space decoding performed within IP-Relay16. The addresses are offsets from the IO space base address.

Programming

Programming IP-Relay16 requires only the ability to read and write data in the host's I/O space. The IP Carrier board determines the base address of this address space. This documentation refers to the base address as the beginning of the I/O space for the slot in which the IP is installed.

Operation of IP-Relay16 is very simple with only the Control Register, Revision and ID. If the NO/NC connections are what is desired no initialization is required since the HW defaults to this condition. To change any particular Relay from not active to active, set the corresponding bit in the control register.

The revision register is provided to allow software to know what version of CPLD program is installed. As new features are added the revision can be useful to determine operation and feature availability.

Dynamic Engineering carrier and module drivers work together to allocate memory to the carrier and the individual IPs plus provide handles to the user level software to gain access. The UserAp reference SW package demonstrates operation of IP-Relay16.

There is enough detail in this manual to write your own driver should that be necessary.

REGISTER DEFINITIONS

Relay Control

$00 IP-Relay16 Control Register Port read/write

Relay Control Register	
DATA BIT	**DESCRIPTION**
15-0	1 = energize relay 0 = non energized

FIGURE 3 IP-RELAY16 RELAY CONTROL BIT MAP

The relays are controlled from this register. Bit(0) = Relay 0, Bit(15) = Relay 15. Register resets to 0x0000.

When each bit is '0' the associated relay is in the non-energized condition. The COM terminal is connected to the NC and NO is open.

When each bit is '1' the associated relay is in the energized condition. The COM terminal is connected to the NO and NC is open.

Check the Relay description table for the switching time to switch to the energized state or vice-versa.

Pinout for IO connector at rear of manual.

Relay Revision

$08 Relay16 Revision Register Port read/write

IO UPPER CONTROL REGISTER	
DATA BIT	**DESCRIPTION**
15-8	Revision Major
7-0	Revision Minor

FIGURE 4 IP-RELAY16 REVISION REGISTER BIT MAP

Revision Major current : x01
Revision Minor current : x01

Initial Release x0101.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-Relay16 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-Relay16-IO board will be recorded with a new code in the DRIVER ID location.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($0E) Relay16
0D	Revision	($01) MajorRev
0F	reserved	($01) Customer Number
11	Driver ID, low byte	($01) Design Number
13	Driver ID, high byte	($01)
15	No of extra bytes used	($0C)
17	CRC	($3F)

FIGURE 5 IP-RELAY16 ID PROM

Loop-back

The Engineering kit has reference software, which includes an external LED Visual test. The test assumes the IP-Debug-IO is connected with the following modifications.

Tie F3P3V to each of the COMs
(49) ⇔ 2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47

Add LEDs to NO0-15 with : NO resistor (RED) A-LED-C GND as the topology
Add LEDs to NC0-15 with : NC resistor (GRN) A-LED-C GND as the topology

Using IP-Debug-IO without test points: Use bus wire to create a ground. Solder the resistor to the (IO) pad and the other end to the LED (A). The Cathode of the LED was then connected to the bus wire.

R0_NO	3	300Ω	-|>|-	bus wire (gnd)
R1_NO	6	300Ω	-|>|-	bus wire (gnd)
R2_NO	9	300Ω	-|>|-	bus wire (gnd)
R3_NO	12	300Ω	-|>|-	bus wire (gnd)
R4_NO	15	300Ω	-|>|-	bus wire (gnd)
R5_NO	18	300Ω	-|>|-	bus wire (gnd)
R6_NO	21	300Ω	-|>|-	bus wire (gnd)
R7_NO	24	300Ω	-|>|-	bus wire (gnd)
R8_NO	27	300Ω	-|>|-	bus wire (gnd)
R9_NO	30	300Ω	-|>|-	bus wire (gnd)
R10_NO	33	300Ω	-|>|-	bus wire (gnd)
R11_NO	36	300Ω	-|>|-	bus wire (gnd)
R12_NO	39	300Ω	-|>|-	bus wire (gnd)
R13_NO	42	300Ω	-|>|-	bus wire (gnd)
R14_NO	45	300Ω	-|>|-	bus wire (gnd)
R15_NO	48	300Ω	-|>|-	bus wire (gnd)

R0_NC	1	300Ω	-|>|-	bus wire (gnd)
R1_NC	4	300Ω	-|>|-	bus wire (gnd)
R2_NC	7	300Ω	-|>|-	bus wire (gnd)
R3_NC	10	300Ω	-|>|-	bus wire (gnd)
R4_NC	13	300Ω	-|>|-	bus wire (gnd)
R5_NC	16	300Ω	-|>|-	bus wire (gnd)
R6_NC	19	300Ω	-|>|-	bus wire (gnd)
R7_NC	22	300Ω	-|>|-	bus wire (gnd)
R8_NC	25	300Ω	-|>|-	bus wire (gnd)
R9_NC	28	300Ω	-|>|-	bus wire (gnd)
R10_NC	31	300Ω	-|>|-	bus wire (gnd)
R11_NC	34	300Ω	-|>|-	bus wire (gnd)
R12_NC	37	300Ω	-|>|-	bus wire (gnd)
R13_NC	40	300Ω	-|>|-	bus wire (gnd)
R14_NC	43	300Ω	-|>|-	bus wire (gnd)
R15_NC	46	300Ω	-|>|-	bus wire (gnd)

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-Relay16. Pins marked n/c below are defined by the specification, but not used on the IP-Relay16. Also see the User Manual for your carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSEL*	4	29
D1	n/c	5	30
D2	MEMSEL*	6	31
D3	n/c	7	32
D4	INTSEL*	8	33
D5	n/c	9	34
D6	IOSEL*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTREG0*	17	42
D14	A4	18	43
D15	n/c	19	44
BS0*	A5	20	45
BS1*	n/c	21	46
n/c	A6	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

FIGURE 6 IP-RELAY16 LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-RELAY16. Also see the User Manual for your carrier board for more information.

R0_NC	R8_COM	1	26
R0_COM	R8_NO	2	27
R0_NO	R9_NC	3	28
R1_NC	R9_COM	4	29
R1_COM	R9_NO	5	30
R1_NO	R10_NC	6	31
R2_NC	R10_COM	7	32
R2_COM	R10_NO	8	33
R2_NO	R11_NC	9	34
R3_NC	R11_COM	10	35
R3_COM	R11_NO	11	36
R3_NO	R12_NC	12	37
R4_NC	R12_COM	13	38
R4_COM	R12_NO	14	39
R4_NO	R13_NC	15	40
R5_NC	R13_COM	16	41
R5_COM	R13_NO	17	42
R5_NO	R14_NC	18	43
R6_NC	R14_COM	19	44
R6_COM	R14_NO	20	45
R6_NO	R15_NC	21	46
R7_NC	R15_COM	22	47
R7_COM	R15_NO	23	48
R7_NO	F3P3V	24	49
R8_NC	GND	25	50

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

FIGURE 7 IP-RELAY16 IO INTERFACE

The Fused +3.3 has a current limit of 500 mA. DGND is normally not connected.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Cables. Be careful to specify cables with properties matching or exceeding your requirements. For low power systems standard ribbon cable is a handy solution. For higher current systems discrete wiring will be required.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. The relay connections are designed to handle power supplies which do not come up together. The maximum ratings for the devices must be observed.

The rest of the IP-Relay16 components must be treated as CMOS – proper handling techniques must be observed. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered.

The Relays are reasonably fast for real-world control and can maintain a 10 mS cycle [worst case on plus worst case off]. Be careful not to exceed the limits of durability by excessive switching.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html]

Ribbon Cable. We offer a high quality ribbon cable assembly with client defined lengths. Please see http://www.dyneng.com/HDRribn50.html

Relay Configurations

IP-Relay16 can be configured to create multiple switch configurations including

Single Relay Functions

•**Form** A **SPST-NO** NO and COM used, open until energized.
•**Form B SPST-NC** NC and COM used, closed until energized
•**Form C SPDT** Break before Make NO, COM, NC used.
NC connected to COM until energized then NO connected to COM.
Delay from break to make is Relay determined.

Dual Relay Functions

•**Form D** Make(B-COM) before Break (A-B via COM)
COMs tied together, NC Relay 0 = A, NO Relay 1 = B
NO relay 0 and NC relay 1 open
Energize with Relay 1 then Relay 0 SW controlled delay
Release with Relay 0 off then Relay 1 off with SW controlled delay
A-COM, A-COM-B, COM-B, A-COM-B, A-COM effective sequence
•**Form E** Break(A-COM), Make(COM-B), Break(B-D)
NO relay 0 tied to COM relay 1, NC Relay 0 = A, NO Relay 0 = B, NC relay 1 = D
NO relay 1 = open
Energize with Relay 0 then Relay 1 SW controlled delay
Release with Relay 1 off then Relay 0 off with SW controlled delay
note: Relay delay time affects some aspects of this topology.
A-COM & B-D, COM-B-D, COM-B, COM-B-D, A-COM & B-D effective sequence
•**Form F** Make(A-COM), Make(A-B)
NO relay 0 tied to COM relay 1, NO Relay 0 = A, NO Relay 1 = B,
NC relay 0 = open, NC relay 1 = open
Energize with Relay 0 then Relay 1 SW controlled delay
Release with Relay 1 off then Relay 0 off with SW controlled delay
Open, A-COM, COM-A-B, A-COM, open effective sequence
•**Form G** Break(A-B), Break(B-C1)
COM relay 0 tied to NC relay 1, NC Relay 0 = A, NC Relay 1 = B,
COM Relay 1 = C1
NO relay 0 = open, NO relay 1 = open
Energize with Relay 0 then Relay 1 SW controlled delay
Release with Relay 1 off then Relay 0 off with SW controlled delay
A-B-COM1, B-COM1, open, B-COM1, A-B-COM1, open effective sequence

•**Form H** Break(A-B), Break(B-C1), Make(C1-D)

COM relay 0 tied to NC relay 1, NC Relay 0 = A, NC Relay 1 = B,
COM Relay 1 = C1, NO relay1 = D
NO relay 0 = open
Energize with Relay 0 then Relay 1 SW controlled delay
Release with Relay 1 off then Relay 0 off with SW controlled delay
A-B-COM1, B-COM1, COM1-D, B-COM1, A-B-COM1 effective sequence
note: Relay delay time affects some aspects of this topology.

•**Form I** Make(B-C0), Break (A-C0), Make (C0-D)

COM relay 0 tied to COM relay 1, NC Relay 1 = A, COM Relay 0 = C0,
NO Relay 0 = B, NO relay1 = D
NC relay 0 = open
Energize with Relay 0 then Relay 1 SW controlled delay
Release with Relay 1 off then Relay 0 off with SW controlled delay
A-C0, B-C0-A, B-C0-D, B-C0-A, A-C0 effective sequence
note: Relay delay time affects some aspects of this topology.

•**Form K** Center off SPDT

COM relay 0 tied to COM relay 1, NC relay 0 tied to NC relay 1
NC Relay 0 = C, NO Relay 0 = A, NO Relay 1 = B
Energize Relay 0 to connect A-C
Energize Relay 1 to connect B-C
Normally both relays are not on at the same time
0 on & 1 off => both off => 1 on and 0 off for a typical sequence.
note: Remember to account for the Relay delay time unless A-B connection is ok in your system.

•**Form L** Break(A-C), Make(B-C), Make(B-D)

NO relay 0 tied to COM relay 1
NC Relay 0 = A, COM Relay 0 = C, NO Relay 0 = B, NO relay 1 = D
NC relay 1 = open
Energize => Relay 0 on, Relay 1 on with SW controlled delay
Release => Relay 1 off, relay 0 off with SW controlled delay
A-C, C-B, C-B-D, C-B, A-C effective sequence
note: Relay delay time affects some aspects of this topology.

•**Form U** Double Make

COM relay 0 tied to COM relay 1
NO Relay 0 = A, COM Relay 0 = C, NO Relay 1 = B
NC relay 0 = open, NC relay 1 = open
Energize => Relay 0 & 1 on simultaneously
Release => Relay 0 & 1 off simultaneously
open, A-B-C, open effective sequence
note: Still tied together and not using C otherwise effectively makes this **Form X**

•**Form V** Double Break

COM relay 0 tied to COM relay 1
NC Relay 0 = A, COM Relay 0 = C, NC Relay 1 = B
NO relay 0 = open, NO relay 1 = open
Energize => Relay 0 & 1 on simultaneously
Release => Relay 0 & 1 off simultaneously
A-B-C, open, A-B-C effective sequence
note: Still tied together and not using C otherwise effectively makes this **Form Y**

•**Form W** Double Break – Double Make

COM relay 0 tied to COM relay 1
NC Relay 0 = A, COM Relay 0 = C, NO Relay 0 = D
NC relay 1 = B, NO relay 1 = E
Energize => Relay 0 & 1 on simultaneously
Release => Relay 0 & 1 off simultaneously
A-B-C, D-C-E, A-B-C effective sequence
note: Still tied together and not using C otherwise effectively makes this **Form Z**

•**DPDT**

NO relay 0 tied to NC relay 1, NC relay 0 tied to NO relay 1
COM relay 0 = C0, COM relay 1 = C1, NC relay 0 = A, NC relay 1 = B
Energize => Relay 0 & 1 on simultaneously
Release => Relay 0 & 1 off simultaneously
C0-A & C1-B, C0-B & C1-A, C0-A & C1-B effective sequence

Triple Relay Functions

•**Form J** Make(A-C0), Make (B-C0), Break (C2-B)

COM relay 0 tied to COM relay 1, NO Relay 1 tied to NC relay 2
COM Relay 0 = C0, NO relay 0 = A, NO relay 1 = B,COM relay 2 = C2
NC relay 0 = open
Energize => Relay 0 on, Relay 1 on, relay 2 on with SW controlled delay
Release => Relay 2 off, Relay 1 off, relay 0 off with SW controlled delay
B-C2, B-C2 & A-C0, C0-A-B-C2, C0-A-B, C0-A-B-C2, B-C2 & A-C0, B-C2 effective sequence
note: Relay delay time affects some aspects of this topology.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-Relay16 is constructed out of 0.062 inch thick High Temperature FR4 material.

Through hole and surface mounting of components are used.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required, however, they are recommended.

Be careful to install the IP "square" to the carrier to insure the IP connector pins are not bent during installation.

In addition, for high vibration systems the relays may need to be glued down. Please contact the factory for this option. The relays are quite rugged – see the table in this manual. The relays have mass (~.75g) and few solder points (5) and may need some help (glue) for the board level to meet the same shock and vibration.

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat dissipation. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-Relay16 design consists of CMOS and relay circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
Internet Address support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Parallel Interface	16 Form C Relays. 60W, 62.5 VA rated switching power. For example 30V and 2A. 4A max. 220VDC / 250VAC
Software Interface:	Relay Control, Revision, and “ID PROM”
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	Word in IO Space (see memory map) Word in ID Space
Access Time:	back-to-back cycles in 375ns (8MHz.) or 94 nS (32 MHz.) to/from FIFO
Wait States:	1
Interrupt:	none
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	High temp Rohs Compliant FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	0.89 W/^{o}C for uniform heat across IP
Power:	Typical 250 mA @ 5V with 8 relays energized. 4.75 – 5.25V, no +/- 12V used
Environmental:	-40 ⇔ +85C rated devices operating 5% – 95% without “CC” option – non condensing See Relay information for vibration and shock

Order Information

IP-Relay16	IP Module with 16 C form relays 16 bit IP interface, 220 VDC 250 VAC 4A Extended Temperature Standard
-ROHS	Add this extension for ROHS compliant assembly. Standard leaded solder used otherwise
-CC	Add Conformal Coating
	http://www.dyneng.com/IP-Relay16.html
Tools for IP-Relay16	IP-Debug-Bus - IP Bus interface extender http://www.dyneng.com/ipdbgbus.html
	IP--Debug-IO - IO connector breakout http://www.dyneng.com/ipdbgio.html
SW	Currently available SW is included with the purchase of IP-Relay16. Please check the webpage for current offerings – typically Win, Linux. Some have VxWorks available for a one time fee.

Glossary

Acronyms and other specialized names and their meaning:

IP Module	IndustryPack Module - establishes common connectors, connections, size and other mechanical features.
IP Control Bus	Control bus between IP Module and Carrier. 8 or 32 MHz reference frequency – user programmable based on IP Module and Carrier combination. All Dynamic Engineering Modules are 32 capable and all carrier IP module positions independently programmable. 6 dedicated address bits with 16 multiplexed address bit available [22 concatonated = 4 MBytes] for memory accesses. 16 bit data bus [in single wide modules]. 4 predecoded spaces allowing 64 registers etc. with the 6 address bits. Interrupts, byte selects available.
IP IO	Second connector on Module for IO independent of control port. Optimal for flow through architecture. User defined. Connected on carrier to external connector.
IDPROM	Manufacturers information for IndustryPack modules. Contains Module speed characteristics, manufacturer, model number and other customized data. x1E is Dynamic Engineering's ID.
CPLD	Complex Programmable Logic Device. One step below FPGA. Frequently with integrated FLASH to configure.
VHDL	VHSIC (Very High Speed Integrated Circuits) Hardware Description Language. Used to describe the implemented design. Compiler uses as input to generate the programming file.
SPDT, DPDT	Single Pole Double Throw, Double Pole Double Throw respectively. Defines switch and relay operation. See examples in IP-Relay16 manual.

nS, uS, mS	nanoseconds, microseconds, milliseconds
UART	Universal Asynchronous Receiver Transmitter. Common serialized data transfer with start bit, stop bit, optional parity, optional 7/8 bit data. Can be over any electrical interface. RS232 and RS422 are most common.
Baud	Used as the bit period for this document. Not strictly correct but is the common usage when talking about UART's.
FIFO	First In First Out Memory
VSWR	Voltage Standing Wave Ratio. Basically a measure of how well a medium will pass a signal at a given frequency. A measure of the reflected energy. 1 is perfect with no power reflected.
JTAG	Joint Test Action Group – a standard used to control serial data transfer for test and programming operations.
TAP	Test Access Port – basically a multi-state port that can be controlled with JTAG [TMS, TDI, TDO, TCK]. The TAP States are the states in the State machine controlled by the commands received over the JTAG link.
TMS	Test Mode State – this serial line provides the state switching controls. '1' indicates to move to the next state, '0' means stay put in cases where delays can happen, otherwise 0,1 are used to choose which branch to take. Due to complexity of state manipulation the instructions are usually precompiled. Rising edge of TCK valid.
TDI	Test Data In - this serial line provides the data input to the device controlled by the TMS commands. For example the data to program the FLASH comes on the TDI line while the commands to the state-machine

	to move through the necessary states comes over TMS. Rising edge of TCK valid.
TCK	Test Clock provides the synchronization for the TDI, TDO and TMS signals
TDO	Test Data Out is the shifted data out. Valid on the falling edge of TCK. Not all states output data.
Packet	Group of characters transferred. When the characteristics of a group of characters is known the data can be stored in packets, transferred as such and the system optimized as a result. Any number of characters can
Packed	When UART characters are always sent/received in groups of 4 allowing full use of host bus / FIFO bandwidth.
UnPacked	When UART characters are sent on an unknown basis requiring single character storage and transfer over the host bus.
MUX	Multiplexor – multiple signals multiplexed to one with a selection mechanism to control which path is active.
Flash	Non-volatile memory used on Dynamic Engineering boards to store FPGA configurations or BIOS.