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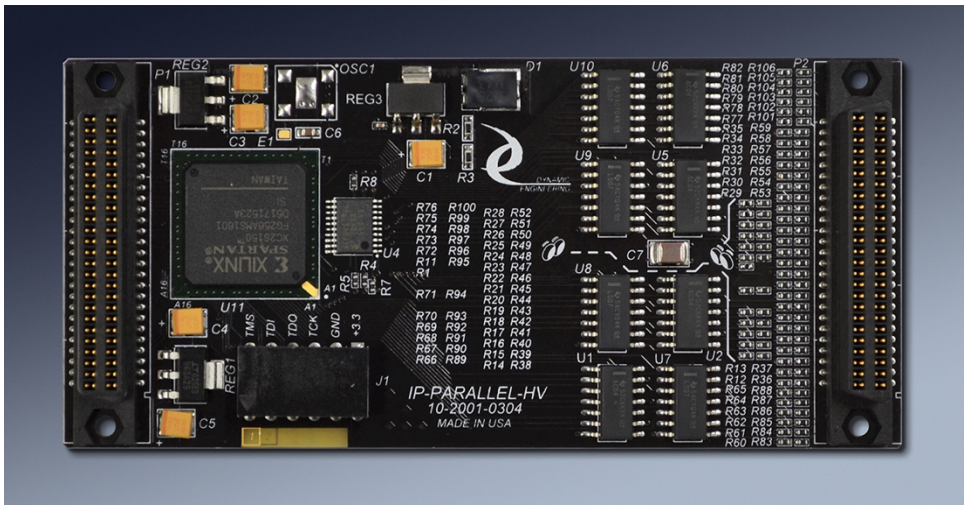
User Manual

IP-HaveQuick

Time Of Day Interface

IndustryPack® Module



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IP-HaveQuick
TOD Interface
IndustryPack® Module

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Table of Contents

List of Figures

Product Description and Operation

IP-HaveQuick formerly known as “IP-Parallel-HQT” is part of the IP Module family of modular I/O components. To receive Time Code, IP-HaveQuick utilizes one 10-volt compatible input (1 PPS) and one 5-volt compatible input (Data). To Transmit, one 10-volt output and one 5-volt output are implemented to source the 1PPS and Data Output.

The outputs utilize LS07’s to provide a high voltage low side switch. The on-board regulator provides the 10V standard reference, and the 5V reference is provided by the IP bus power. Other voltages can be supplied up to 12V. An external supply can be used when desired or if voltages above 12V need to be generated. Each input channel has a resistor divider to scale the input voltage back to “TTL” levels. The resistors can be altered for other voltage requirements.

IP-HaveQuick is designed to receive Have Quick Time data at a rate of approximately 1667 bits/second. The data is Manchester encoded BCD with a modified Hamming code that uses four data bits and four check bits for each decimal digit of the time code. The Manchester encoded data defines a one with 300 microseconds of a high level followed by 300 microseconds of a low level. A zero has the same timing with opposite definitions.

The time transmission occurs once per second and begins with the leading edge of a 10-volt 20-microsecond pulse on input line 0. The Manchester data, which is received on input line 12, begins with 400 bits of one followed by a 16-bit sync code. This is followed by the time data, which consists of a two-digit hour field, a two-digit minute field, a two-digit second field, a three-digit day of year field, a two-digit year field, and a one-digit time-figure-of-merit field. All data except the sync word are binary coded decimal digits preceded by four parity bits per digit. The default sync word is 0x11e9, and this is programmable to any non-zero value.

New with release 3.2 the data is sent MSB first unless the LsbFirst control bit is set. The standard interface is MSB first. Setting the LsbFirst bit changes the Parity Data combination to be bit reversed on a per byte basis. Both Transmitter and Receiver are affected by the selection. The leading ones and sync pattern are not affected by the selection. The default is MSB first.

Output line 0 provides the 20-microsecond 10-volt pulse once per second and output line 12 provides the Manchester time code data. The initial time values are set in a series of registers, one for each field of the time code. Once started the values automatically increment to provide the proper time.

Four interrupt sources are provided: transmission completion, reception completion, receive parity error, and receive framing error. The framing error is asserted if the number of one-bits received before the sync word is not 400, or if the transmission terminates before the entire time code is received. The parity error is asserted if the parity bits for a particular digit do not match the expected value for that digit. The interrupts can be individually enabled and a master interrupt enable is also provided. The interrupt occurs on IntReq0. The vector can be read in the IO space or automatically with the INT space select strobe.

IP-HaveQuick supports both 8 and 32 MHz. IP Bus operation. All configuration registers support read and write operations for maximum software convenience. The ID, IO, and INT spaces are utilized by the IP-Parallel-HQT design, but not the MEM space. It is important to select the proper state of the selection in the Base Resister – the 1PPS width is determined by counting IP clocks and will be the wrong width if not selected to match the carrier setting.

IP-HaveQuick conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. The PCIe3IP carrier makes a convenient development platform in many cases.
http://www.dyneng.com/PCIe3IP.html
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Address Map

Function	Offset	Width	Type	Function
IPHQT_BASE_CONTROL	0x0000	word	read/write	Base control register
IPHQT_TX_CONTROL	0x0002	word	read/write	Time code transmit control
IPHQT_RX_CONTROL	0x0004	word	read/write	Time code receive control
IPHQT_YEAR	0x0006	word	read/write	Year pre-load value
IPHQT_DAY_OF_YEAR	0x0008	word	read/write	DayOfYear pre-load value
IPHQT_HOUR	0x000A	word	read/write	Hour pre-load value
IPHQT_MINUTE	0x000C	word	read/write	Minute pre-load value
IPHQT_SECOND	0x000E	word	read/write	Second pre-load value
IPHQT_SYNC_WORD	0x0010	word	read/write	Sync word register
IPHQT_LOAD_TIME	0x0012	word	write only	Load time register values
IPHQT_READ_DATA_0	0x0014	word	read only	Fraction of second -> 16-bits
IPHQT_READ_DATA_1	0x0016	word	read only	Bits 15..0 of time data
IPHQT_READ_DATA_2	0x0018	word	read only	Bits 31..16 of time data
IPHQT_READ_DATA_3	0x001A	word	read only	Bits 47..32 of time data
IPHQT_READ_FIFO_0	0x001C	word	read only	Bits 15..0 of time FIFO data
IPHQT_READ_FIFO_1	0x001E	word	read only	Bits 31..16 of time FIFO data
IPHQT_READ_FIFO_2	0x0020	word	read only	Bits 47..32 of time FIFO data
IPHQT_READ_FIFO_3	0x0022	word	read only	FIFO sample count -> 16-bits
IPHQT_STATUS	0x0024	word	read only	Status register
IPHQT_VECTOR	0x002C	word	read/write	Vector register
IPHQT_IDPROM	idsel	byte on word boundary		Module ID (read only)

FIGURE 1 IP-HAVEQUICK INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-HaveQuick. The addresses are all offsets from a base address provided by the carrier board in which the IP is installed.

Programming

Programming the IP-HaveQuick requires only the ability to read and write data in the host's I/O space. The IP Carrier board determines the base address of the module.

In order to read the time data the user can read real-time data from four consecutive registers, which includes a 16-bit fractional second count that is synchronized to the one-second pulse. Each count of this register equals 1/10,000 of a second (100 microseconds). In order to coordinate the whole second count with the fractional second count, the received time code is not available to be read until the following one-second pulse. If the Windows driver is used to control the board, it will automatically increment the time read by one second to reconcile this difference.

There is also a 512 by 64-bit FIFO that stores time code samples as they are received. The FIFO word includes a 16-bit sample count that increments with each sample received. The sample count can be cleared and the FIFO can be reset with separate control bits in the receive control register.

The initial time value sent by the transmit section can be specified in a series of registers described below. Once these values have been written, a dummy write to the IPHQT_LOAD_TIME port transfers all the values into the transmitter at once. The sync word register is used by both the receive and transmit functions. If this register is programmed to zero [illegal value] (the power-up state), the default value 0x11e9 will be used instead.

Please note: whether using standard or LsbFirst mode the Sync pattern is always sent MSB first. If your application needs the sync to be broadcast LSB first the register will need to be programmed with reversed bit order.

Register Definitions

IPHQT_BASE_CONTROL

0x0000 Base control register port read/write

BASE CONTROL REGISTER

DATA BIT	DESCRIPTION
15-12	Time figure of merit value to transmit
11-5	spare
4	LsbFirst
3	Spare
2	force interrupt 1 = force
1	master interrupt enable 1 = enabled
0	IP clock flag 1 = 32MHz, 0 = 8MHz

FIGURE 2 IP-HAVEQUICK BASE CONTROL REGISTER BIT MAP

IP clock flag: This bit is utilized by the various timing signals in HaveQuick to ensure the proper divide-by value is used. Set when the Carrier supplied IP reference clock is 32 MHz and clear when operating at 8 MHz.

Master interrupt enable: This bit when zero disables all interrupts. It is used in the interrupt service routine to stop interrupts and must be re-enabled to continue interrupt processing.

Force interrupt: This bit is used to cause an interrupt with software in order to develop interrupt routines and test hardware interrupt paths. Also useful for BIT.

LsbFirst: When set the payload of the message is transmitted with each byte bit reversed for Lsb first operation. Within the payload each byte is formed with Parity and Data – 1 nibble of each. In standard mode the data is sent P3P2P1P0D3D2D1D0. With LsbFirst set the pattern shifts to D0D1D2D3P0P1P2P3. Time of Day plus Figure of Merit are affected.

Time figure of merit: This value is appended to the end of the time transmission and can be set to any value from 0 to 9.

IPHQT_TX_CONTROL

0x0002 Transmit Control Register Port read/write

TRANSMIT CONTROL REGISTER	
DATA BIT	**DESCRIPTION**
15-5	spare
4	Tx interrupt enable 1 = enabled, 0 = disabled
3-1	spare
0	Tx run 1 = send time data, 0 = stop

FIGURE 3 IP-HAVEQUICK TX CONTROL BIT MAP

Tx run: This bit when set ‘1’ starts the one-second pulse and time code transmission.

Tx interrupt enable: This bit when set ‘1’ enables the transmit interrupt. This interrupt will be asserted upon the completion of a time code transmission. When cleared ‘0’ transmit interrupts are disabled. Requires the Master Interrupt Enable to be Enabled.

IPHQT_RX_CONTROL

0x0004 Receive Control Register Port read/write

RECEIVE CONTROL REGISTER	
DATA BIT	**DESCRIPTION**
15-7	spare
6	Rx frame error interrupt enable 1 = enabled
5	Rx parity error interrupt enable 1 = enabled
4	Rx data received interrupt enable 1 = enabled
3	spare
2	Clear FIFO 1 = FIFO reset, 0 = normal operation
1	Sample count clear 1 = reset, 0 = count samples
0	Rx start 1 = start, 0 = stop

FIGURE 4 IP-HAVEQUICK RX CONTROL BIT MAP

Rx start: When set ‘1’, reception and storage of time codes is enabled. When cleared ‘0’, time code reception is halted.

Sample count clear: Set ‘1’ then clear ‘0’ to reset the sample counter. This 16-bit count is added to the time code data stored in the sample FIFO.

Clear FIFO: Set ‘1’ then clear ‘0’ to reset the sample FIFO. This will purge all data, set the data count to zero, and assert the FIFO empty flag.

The Rx interrupt functions also require the Master Interrupt Enable.

Rx interrupt enable: When set ‘1’ enables the receiver interrupt. This interrupt will be asserted upon the completion of a time code reception. When cleared ‘0’, receive interrupts are disabled.

Rx parity error interrupt enable: When set ‘1’ enables an interrupt to be asserted when a receive parity error is detected. The four parity bits received with each digit of the time code are compared to the expected value for the digit received. If these values do not match, a parity error is latched. When this bit is ‘0’, the parity error can not cause an interrupt, but the status is still latched and can be read at any time.

Rx frame error interrupt enable: When set ‘1’ enables an interrupt to be asserted when a framing error is detected. Set when the initial count of 1s is not 400. A framing error is also asserted if the transmission stops before the complete time code is received. When this bit is ‘0’, the frame error can not cause an interrupt, and the status is still latched and can be read allowing polled operation.

IPHQT_YEAR

0x0006 Year Register Port read/write

YEAR DEFINITION REGISTER	
DATA BIT	**DESCRIPTION**
15-8	spare
7-4	Year most significant digit (BCD)
3-0	Year least significant digit (BCD)

FIGURE 5 IP-HAVEQUICK YEAR BIT MAP

The initial value for the year field is entered in this register. Each digit of the two-digit year field is represented by a four-bit binary coded decimal.

IPHQT_DAY_OF_YEAR

0x0008 Day of Year Register Port read/write

DAY OF YEAR DEFINITION REGISTER	
DATA BIT	**DESCRIPTION**
15-12	spare
11-8	Day of Year most significant digit (BCD)
7-4	Day of Year second digit (BCD)
3-0	Day of Year least significant digit (BCD)

FIGURE 6 IP-HAVEQUICK DAY OF YEAR BIT MAP

The initial value for the day of year field is entered in this register. Each digit of the three-digit day of year field is represented by a four-bit binary coded decimal.

IPHQT_HOUR

0x000A Hour Register Port read/write

HOUR DEFINITION REGISTER	
DATA BIT	**DESCRIPTION**
15-8	spare
7-4	Hours most significant digit (BCD)
3-0	Hours least significant digit (BCD)

FIGURE 7 IP-HAVEQUICK HOUR BIT MAP

The initial value for the hour field is entered in this register. Each digit of the two-digit hour field is represented by a four-bit binary coded decimal.

IPHQT_MINUTE

0x000C Minute Register Port read/write

MINUTE DEFINITION REGISTER	
DATA BIT	**DESCRIPTION**
15-8	spare
7-4	Minutes most significant digit (BCD)
3-0	Minutes least significant digit (BCD)

FIGURE 8 IP-HAVEQUICK MINUTE BIT MAP

The initial value for the minute field is entered in this register. Each digit of the two-digit minute field is represented by a four-bit binary coded decimal.

IPHQT_RX_SECOND

0x000E Second Register Port read/write

SECOND DEFINITION REGISTER	
DATA BIT	**DESCRIPTION**
15-8	spare
7-4	Seconds most significant digit (BCD)
3-0	Seconds least significant digit (BCD)

FIGURE 9 IP-HAVEQUICK SECOND BIT MAP

The initial value for the second field is entered in this register. Each digit of the two-digit second field is represented by a four-bit binary coded decimal.

IPHQT_SYNC_WORD

0x0010 Sync Word Register Port read/write

SYNC WORD DEFINITION REGISTER	
DATA BIT	**DESCRIPTION**
15-0	Sync word value (16 bits)

FIGURE 10 IP-HAVEQUICK SYNC WORD BIT MAP

The 16-bit sync word is used by both the transmit and receive function. The receiver compares this value to the incoming bit stream to determine where the time data begins. The transmitter sends this code in the proper position in the bit stream so that the code will be recognized. If a zero value is written to this register (or on power-up) a value of 0x11e9 will be used instead.

IPHQT_LOAD_TIME

0x0012 Load Initial Transmit Time write only

A write of any value to this address offset will cause the values in the above time code registers to be loaded into the transmitter. These values will be the first time shifted out of the transmitter. Subsequent times will each be incremented by one second.

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IPHQT_READ_DATA_0

0x0014 Read Real-Time Data Port0 read only

READ TIME DATA 0	
DATA BIT	**DESCRIPTION**
15-0	Fractional second count

FIGURE 11 IP-HAVEQUICK READ DATA 0 BIT MAP

Each count in this register represents 1/10,000 second (100 microseconds). The count is reset when the one-second pulse is received.

IPHQT_READ_DATA_1

0x0016 Read Real-Time Data Port1 read only

READ TIME DATA 1	
DATA BIT	**DESCRIPTION**
15-12	Day of year least significant digit (BCD)
11-8	Year most significant digit (BCD)
7-4	Year least significant digit (BCD)
3-0	Time figure of merit digit (BCD)

FIGURE 12 IP-HAVEQUICK READ DATA 1 BIT MAP

IPHQT_READ_DATA_2

0x0018 Read Real-Time Data Port2 read only

READ TIME DATA 2	
DATA BIT	**DESCRIPTION**
15-12	Seconds most significant digit (BCD)
11-8	Seconds least significant digit (BCD)
7-4	Day of year most significant digit (BCD)
3-0	Day of year second digit (BCD)

FIGURE 13 IP-HAVEQUICK READ DATA 2 BIT MAP

IPHQT_READ_DATA_3

0x001A Read Real-Time Data Port3 read only

READ TIME DATA 3	
DATA BIT	**DESCRIPTION**
15-12	Hours most significant digit (BCD)
11-8	Hours least significant digit (BCD)
7-4	Minutes most significant digit (BCD)
3-0	Minutes least significant digit (BCD)

FIGURE 14 IP-HAVEQUICK READ DATA 3 BIT MAP

The values in these four registers were received before the previous one-second pulse. In order to coordinate the fractional second count with the rest of the time values, the received value is not available to be read until the next one-second pulse. This ensures that subsequent reads will always return increasing values. If our driver is used to communicate with the board, it will automatically add one second to the time value read, carrying this increment up through the more significant fields as necessary.

IPHQT_READ_FIFO_0

0x001C Read Stored Data Port0 read only

READ TIME DATA FIFO 0	
DATA BIT	**DESCRIPTION**
15-12	Day of year least significant digit (BCD)
11-8	Year most significant digit (BCD)
7-4	Year least significant digit (BCD)
3-0	Time figure of merit digit (BCD)

FIGURE 15 IP-HAVEQUICK READ FIFO 0 BIT MAP

IPHQT_READ_FIFO_1

0x001E Read Stored Data Port1 read only

READ TIME DATA FIFO 1	
DATA BIT	**DESCRIPTION**
15-12	Seconds most significant digit (BCD)
11-8	Seconds least significant digit (BCD)
7-4	Day of year most significant digit (BCD)
3-0	Day of year second digit (BCD)

FIGURE 16 IP-HAVEQUICK READ FIFO 1 BIT MAP

IPHQT_READ_FIFO_2

0x0020 Read Stored Data Port2 read only

READ TIME DATA FIFO 2	
DATA BIT	**DESCRIPTION**
15-12	Hours most significant digit (BCD)
11-8	Hours least significant digit (BCD)
7-4	Minutes most significant digit (BCD)
3-0	Minutes least significant digit (BCD)

FIGURE 17 IP-HAVEQUICK READ FIFO 2 BIT MAP

IPHQT_READ_FIFO_3

0x0022 Read Stored Data Port3 read only

READ TIME DATA FIFO 3	
DATA BIT	**DESCRIPTION**
15-0	FIFO sample count

FIGURE 18 IP-HAVEQUICK READ FIFO 3 BIT MAP

The values in these four registers are stored as soon as they are received. For each time code received the sample count is incremented. If the FIFO fills up, no more data will be written into it, but the sample count will continue to increment with every time code reception.

IPHQT_STATUS

0x0024 Status Port read/write

STATUS REGISTER	
DATA BIT	**DESCRIPTION**
15	Interrupt request 1 = active, 0 = inactive
14	Interrupt status 1 = enabled interrupt condition exists
13-12	Spare
11	Load Time Latched
10	spare
9	FIFO data valid 1 = data ready, 0 = data not ready
8	Real-time data valid 1 = data ready, 0 = data not ready
7	FIFO full 1 = full, 0 = not full
6	FIFO half full 1 = half full or more, 0 = below half full
5	FIFO quarter full 1 = quarter full, 0 = not quarter full
4	FIFO empty 1 = empty, 0 = not empty
3	Rx frame error latched
2	Rx parity error latched
1	Rx complete interrupt latched
0	Tx complete interrupt latched

FIGURE 19 IP-HAVEQUICK STATUS REGISTER BIT MAP

Tx complete interrupt latched: When a time code transmission completes this bit is set to a one. It is cleared by writing bit 0 to the Status port address.

Rx complete interrupt latched: When a time code reception completes this bit is set to a one. It is cleared by writing bit 1 to the Status port address.

Load Time Latched: When data is stored into the Time Code Receive Registers this bit is set to a one. It is cleared by writing bit 11 to the Status port address. This bit can be polled to determine when data is valid. Added with 3p2 flash.

Rx parity error latched: When a parity error is detected in a time code reception this bit is set to a one. It is cleared by writing bit 2 to the Status port address.

Rx frame error latched: When a frame error is detected in a time code reception this bit is set to a one. It is cleared by writing bit 3 to the Status port address.

FIFO empty: When the sample FIFO is empty this bit will be read as a one. If the FIFO has any data in it, this bit will be read as a zero.

FIFO quarter full: When the sample FIFO is greater or equal to ¼ full but less than half

full or if it is greater or equal to ¾ full this bit will be read as a one. If the FIFO is below ¼ full or between half full and ¾ full, this bit will be read as a zero.

FIFO half full: When the sample FIFO is greater or equal to ½ full this bit will be read as a one. If the FIFO is below half full, this bit will be read as a zero.

FIFO full: When the sample FIFO is full this bit will be read as a one. If the FIFO has room for any more data in it, this bit will be read as a zero.

Real-time data valid: When the first time code is received after the receiver is enabled, this bit will be set to a one. After that the bit is only cleared when the receiver is disabled. Recommend using Load Time Latched bit instead. This bit remains to support previously delivered systems.

FIFO data valid: This bit is still provided and reflects the Empty condition Rev 3p2 and later.

Interrupt status: When this bit is read as a one, it indicates that an enabled interrupt condition is active, however an interrupt will only be asserted if the master interrupt enable is also set. When this bit is read as a zero, it means that no enabled interrupt condition exists.

Interrupt request: When this bit is read as a one, it indicates that a system interrupt is asserted. This means that Interrupt status is true and the master interrupt is enabled. When this bit is read as a zero, it means that either no enabled interrupt condition exists or the master interrupt is disabled or both.

IPHQT_VECTOR

0x002C IP-Parallel-HQT Interrupt Vector Port read/write

The Interrupt vector for the IP-Parallel-HQT is stored in this byte wide register, which is initialized to '0xFF' upon power-on reset. The vector is stored in the odd byte location [D7..0].

Interrupts

All IP Module interrupts are potentially vectored. Some carriers and SW packages treat the interrupt as Auto-Vectored. If using the vectored interrupts, the vector register needs to be loaded as part of the initialization process. The vector register can be programmed to any 8-bit value. The default value $FF is sometimes not a valid user vector. Software is responsible for choosing a valid user vector if necessary. Most PCI/PCIe devices do not use the vector while VME and other architectures do.

For vectored interrupts, IP-HaveQuick generates an interrupt request when an enabled interrupt condition is detected. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector when accessed by the CPU. The source of the interrupt is obtained by reading the IPHQT_STATUS register.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the IPHQT_BASE_CONTROL register. The individual interrupt enables are controllable through the IPHQT_TX_CONTROL and IPHQT_RX_CONTROL registers. The enable operates after the interrupt holding latch, which stores the request for the CPU. Once the interrupt condition is latched, the way to clear the latch is to write the same bit back to the status register. The Interrupt acknowledge cycle fetches the vector, and clears the interrupt latch if the driver is used.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision to be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-HaveQuick is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-HaveQuick board will be recorded with a new code in the DRIVER ID and reserved fields.

Address	Data Type	Value
01	ASCII "I"	$49
03	ASCII "P"	$50
05	ASCII "A"	$41
07	ASCII "H"	$48
09	Manufacturer ID	$1E
0B	Model Number	$04
0D	Revision	$A0
0F	reserved	$01
11	Driver ID, low byte	$02
13	Driver ID, high byte	$00
15	No of extra bytes used	$0C
17	CRC	$15

FIGURE 20 IP-HAVEQUICK ID PROM

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on IP-HaveQuick. Pins marked n/c below are defined by the specification, but not used on the IP-HaveQuick. See the User Manual for your carrier board for more information.

GND		GND	1	26	
	CLK	+5V	2		27
Reset*		R/W*	3	28	
	D0	IDSEL*	4		29
D1		DMAReq0*	5	30	
	D2	MEMSEL*	6		31
D3		DMAReq1*	7	32	
	D4	IntSel*	8		33
D5		DMAck*	9	34	
	D6	IOSel*	10		35
D7		n/c	11	36	
	D8	A1	12		37
D9		DMAEnd*	13	38	
	D10	A2	14		39
D11		n/c	15	40	
	D12	A3	16		41
D13		IntReq0*	17	42	
	D14	A4	18		43
D15		IntReq1*	19	44	
	BS0*	A5	20		45
BS1*		n/c	21	46	
	n/c	A6	22		47
n/c		Ack*	23	48	
	+5V	n/c	24		49
GND		GND	25	50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. This table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked in the silk-screen.

FIGURE 21 IP-HAVEQUICK LOGIC INTERFACE

IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the I IP-HaveQuick. Also see the User Manual for your carrier board for more information.

O_0	Pulse out	I_0	Pulse in	1		26	
	O_1		I_1		2		27
O_2		I_2		3		28	
	O_3		I_3		4		29
O_4		I_4		5		30	
	O_5		I_5		6		31
O_6		I_6		7		32	
	O_7		I_7		8		33
O_8		I_8		9		34	
	O_9		I_9		10		35
O_10		I_10		11		36	
	O_11		I_11		12		37
O_12	Time data out	I_12	Time data in	13		38	
	O_13		I_13		14		39
O_14		I_14		15		40	
	O_15		I_15		16		41
O_16		I_16		17		42	
	O_17		I_17		18		43
O_18		I_18		19		44	
	O_19		I_19		20		45
O_20		IO_20		21		46	
	O_21		I_21		22		47
O_22		I_22		23		48	
	O_23		I_23		24		49
VIO		GND		25		50	

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. This table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked in the silk-screen. Unused pins should not be connected.

FIGURE 22 IP-HAVEQUICK IO INTERFACE

VIO is used to source 10 V in this design. The DIODE coupling allows external voltages to be connected to IP-HaveQuick without modification to the card. The external voltage must be greater than the reference voltage. With changes to the regulator settings [resistors] the onboard regulator can be “programmed” for other reference voltages [12 V max output]

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the IP-HaveQuick when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. The open collector drivers can handle relatively large offsets in voltage and are designed to operate when parts of the system are powered and parts are not. IP-HaveQuick does contain resistive input protection. It is better design practice to keep the voltage offsets minimized, and the potential for current flowing though un-powered electronics to a minimum.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html] Dynamic Engineering also stocks ribbon cable in a variety of lengths. http://www.dyneng.com/HDRribn50.html

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

Loop-back Connections

The ATP software we use to test the IP-HaveQuick includes a loop-back test. The Engineering Kit for the IP-HaveQuick includes the source code for the ATP. The loop-back test is facilitated with an IP-Debug-IO card with added wire-wrapped interconnections.

Model “HQT”

To	From	Signals	Function
26	1	I0 - O0	1-second Pulse
38	13	I12 – O12	Have Quick Time Data

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-HaveQuick is constructed out of 0.062" thick high temperature ROHS compliant FR4 material.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. IP-HaveQuick comes with the IP side HW. Dynamic Engineering carriers are provided with the standoffs already installed. If you need additional HW IP-MTG-KIT is available.
http://www.dyneng.com/IPHardware.html

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-HaveQuick design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St Suite C
Santa Cruz, CA 95060
831-457-8891
support@dyneng.com

Specifications

Logic Interface:	IP Module Logic Interface
Parallel Interface:	2 open collector outputs. 30 mA sink with 470Ω pull-up to reference Voltage. 2 Inputs with resistor dividers. 10V(1 PPS) and 5V(HQT) expected Standard reference voltage of 6.5V
Software Interface:	Control Registers, ID PROM, Vector Register, Status Port
Initialization:	Hardware Reset forces all registers except vector register to 0.
Access Modes:	Word I/O Space (see memory map) Word in ID Space Vectored interrupt
Wait States:	1 to all spaces
Interrupt:	Four interrupt conditions specified.
DMA:	No Logic Interface DMA Support implemented at this time.
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface [HDRterm50] User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	High temp ROHS compatible FR4 Multi-Layer Printed Circuit, Through Hole and SMT
Temperature Coefficient:	0.89 W/^{O}C for uniform heat across IP
Power:	Max. **TBD** mA @ 5
MTBF	1.855 M Hours GB 25C Bellcore

Order Information

IP-HaveQuick.
https://www.dyneng.com/IP-HaveQuick.html

"**HQT"**	IP Module with HaveQuick interface. Receive and transmit independent. 8 and 32 MHz operation. Multiple interrupt and polling options. Supported with Win10 IP module driver plus DynEngCarrier driver package.
-ROHS	Add ROHS processing. Standard is leaded solder.
Tools for IP-HaveQuick	IP-Debug-Bus - IP Bus interface extender with testpoints, isolated power and quickswitch technology to allow hot swapping of IPs or power cycling without powering down the host. https://www.dyneng.com/ipdbgbus.html
	IP-Debug-IO II - IndustryPack IO connector breakout with testpoints, ribbon cable headers, and locations for user circuits. https://www.dyneng.com/ipdbgio.html
	HDRterm50 - Ribbon cable compatible 50 pin header to 50 screw terminal header. Comes with DIN rail mounting capability. https://www.dyneng.com/HDRterm50.html
	PCIe3IP - 1/2 length PCIe card with 3 IP slots. https://www.dyneng.com/PCIe3IP.html