DD-03282

ARINC 429 TRANSCEIVER

DESCRIPTION

The DD-03282 device is a two-channel receiver, one-channel transmitter in accordance with the "ARINC Specification 429 Digital Information Transfer System, Mark 33" (ARINC 429). This device can be used in conjunction with the DD-03182 Line Driver chip.

The DD-03282 provides an interface between a standard avionics type serial digital data bus and 16-bit-wide digital data buses. The interface circuit consists of a transmitter circuit, two iden-tical but independent receiver circuits, and a programmable control register to select operating options. The two receiver circuits operate identically. Each contains a line receiver which provides a direct electrical interface to an ARINC 429 data bus.

The Transceiver transmits TTL information on DO(A)/DO(B) output pins. The signal format is compatible with DDCs ARINC-429 line driver chip DD-03182.

FEATURES

- ***Harris/Holt/Raytheon Pin-for-Pin Alternate for Most Applications****
- ***Two Receivers & One Transmitter***
- ***Parity Status & Generation of Receive and Transmit Words***
- ***Wraparound Self Test***
- ***Low Power CMOS***

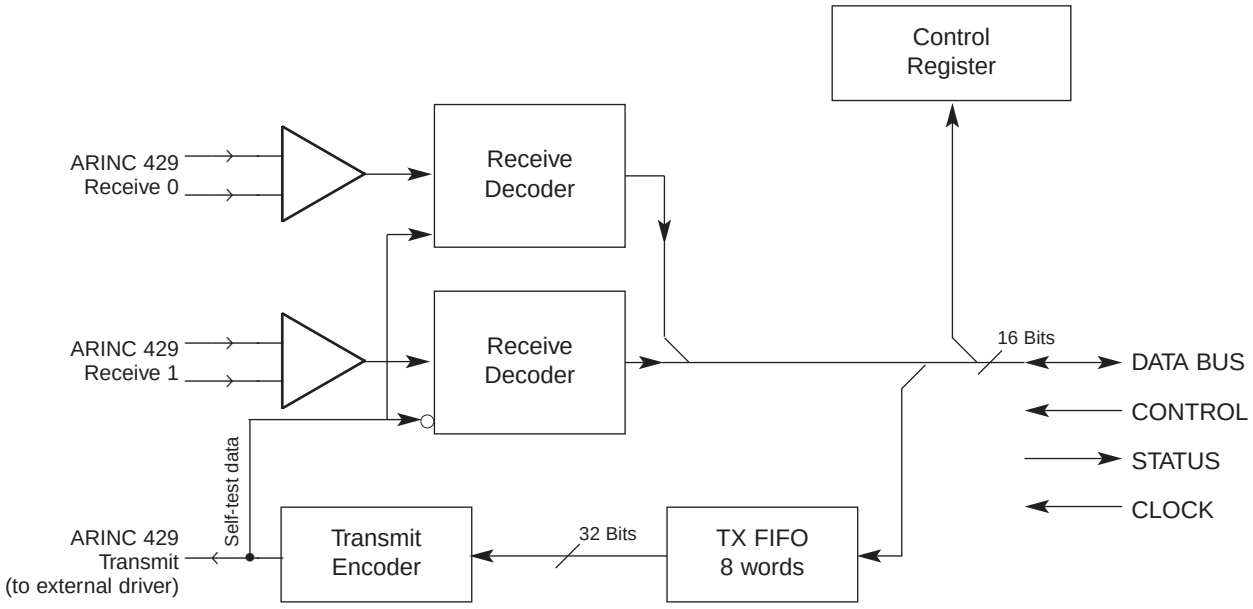


FIGURE 1. DD-03282 BLOCK DIAGRAM

* Reference Application Note AN/A-5.

TABLE 1. DD-03282 SPECIFICATION
ELECTRICAL DESCRIPTION (MAXIMUM RATINGS)

Supply Voltage (V_{CC})	- 0.5V to + 7.0V
DC Input Voltage (V_{IN}) (except pinsDI1+2(A + B))	-1.5V to V_{CC} + 1.5V
Voltage at Pins DI1(A,B) and DI2(A,B)	-29V to + 29V
Clamp Diode Current	± 20 mA
DC Output Current, per pin	± 25 mA
DCV or GND current, per pin	± 50 mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
1MCK Clock Frequency	1.16 MHz

TABLE 2. DD-03282 SPECIFICATION
DC ELECTRICAL CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
	ARINC LINE INPUTS					
V_{IH}	Logic 1 Input Voltage	6.5	10	13	V	V_{DIFF} PIN 2-3, 4-5
V_{IL}	Logic 0 Input Voltage	-6.5	-10	-13	V	V_{DIFF} PIN 2-3, 4-5
V_{NUL}	Null Input Voltage	-2.5	0	+2.5	V	V_{DIFF} PIN 2-3, 4-5
V_{CM}	Common Mode Voltage			±5	V	
R_I	Differential Input Impedance	6			Kohm	
R_H R_G	Input Impedance to V_{CC} Input Impedance to GND	12 12			Kohm Kohm	
C_I	Differential Input Capacitance			20	pF	
C_H	Input Capacitance to V_{CC}			20	pF	
C_G	Input Capacitance to GND			20	pF	
	ALL OTHER INPUTS (including bidirectional)					
V_{IL}	Max. Low Level Input Voltage			0.8	V	
V_{IH}	Min. High Level Input Voltage	2.0			V	
I_{IN}	Max. Input Current			±10	µA	V_{IN} = GND to V_{CC}
C_{IN}	Input Capacitance			15	pF	
	ALL OUTPUTS (including bidirectional)					
V_{OH}	Min. High Level Output Voltage	V_{CC} -0.1 2.7			V V	$\|I_{OUT}\|$ = 20µA $\|I_{OUT}\|$ = 6mA
V_{OL}	Max. Low Level Voltage			0.1 0.4	V V	$\|I_{OUT}\|$ = 20µA $\|I_{OUT}\|$ = 6mA
I_{CC}	Supply Current		5.0	10	mA	1MCK = 1MHz
V_{CC}	Supply Voltage	4.5	5.0	5.5	VDC	

TABLE 3. DD-03282 SPECIFICATION
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	DATA RATE 100 kb/s MIN	DATA RATE 100 kb/s MAX	DATA RATE 12.5 kb/s MIN	DATA RATE 12.5 kb/s MAX	UNITS
CK_{DC}	1MCK Duty Cycle	40	60	40	60	%
T_{CRF}	1MCK Rise/Fall Time		10		10	ns
T_{MR}	Master Reset Pulse Width	200		200		ns
T_{DR}	Transmitter Data Rate (1MCK = 1 MHz)	99	101	12.4	12.6	kbps
R_{DR}	Receiver Data Rate (1MCK = 1 MHz)	95	105	9.0	14.5	kbps

GENERAL DESCRIPTION

ARINC 429, as defined and described in ARINC Specification 429 Digital Information Transfer System, Mark 33, has been in use since 1977. It is the foundation for digital communications in modern civil aircraft. Certification issues have driven 429 to be defined as a simplex bus (one transmitter, multiple receivers) for point-to-point communications using 32-bit words with odd parity and 12-14.5 kHz (Lo Speed) or 100 kHz (Hi Speed) operation.

The DD-03282 provides an interface between a standard avionics type serial digital data bus and most typical 16-bit-wide microcomputer data buses. The avionics buses supported by this device include:

ARINC 429

ARINC 571

ARINC 575

ARINC 706

Delco IRS 9600 Baud Data Bus

ARINC 561 (with support circuitry)

The interface circuit consists of a transmitter circuit, two identical, but independent receiver circuits, and a user-programmable control register for use in selecting operating options. The transmitter circuit contains an 8 word x 32 bit buffer and control logic which allows the user to write a block of data into the transmitter. Once the user enables the transmitter, the data block is automatically sent without further attention.

Two receiver circuits each operate identically. Each contains a line receiver which provides a direct electrical interface to an ARINC-429 data bus. Incoming data is shifted into a 32-bit shift register and latched into a data buffer if a valid word is received. The control register allows the user to select the various options. These include:

Word length (32 or 25 bits).

Transmitter Bit 32 (parity or data).

Transmitter parity (even or odd).

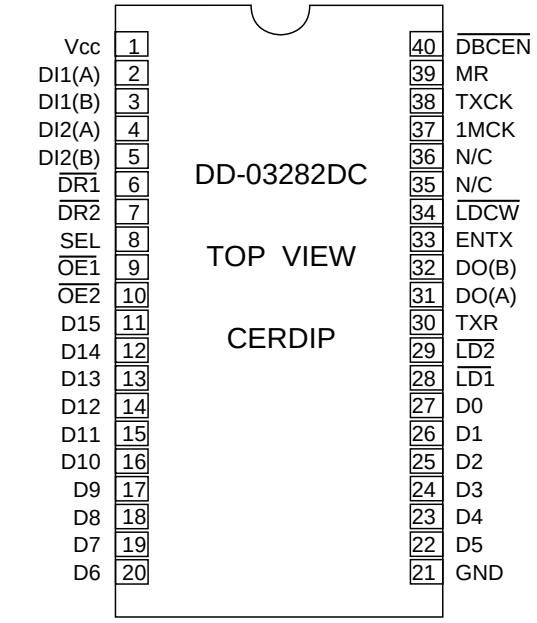
Wraparound self test.

Source/Destination code filtering of received data.

Transmitter data rate (Hi Speed or Lo Speed).

Receiver data rate (Hi Speed or Lo Speed).

The Transceiver fully supports the ARINC 429 data rates and receiver electrical characteristics over temperature (-55° C to +125° C) and voltages (4.5 VDC to 5.5 VDC). It interfaces with TTL, CMOS, or NMOS support circuitry using a standard 5 volt Vcc supply.



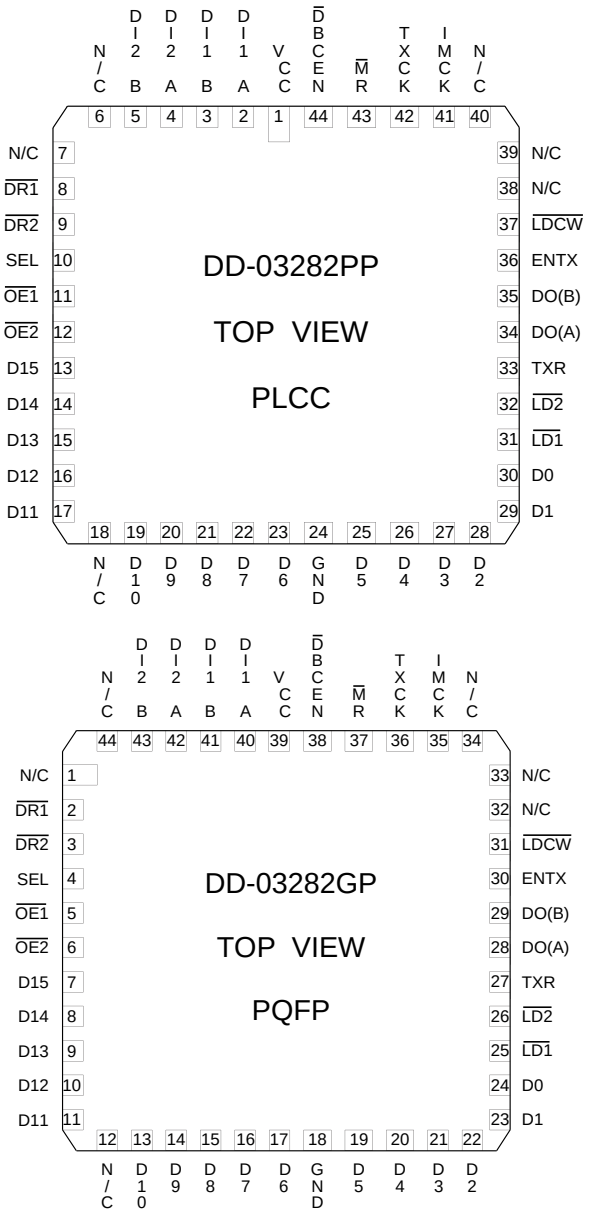


FIGURE 2. DD-03282 PIN-OUT

PIN DESCRIPTIONS (Refer to FIGURE 2)

Vcc	5 VDC power input.
DI1(A)	Data In 1, HI (input, ARINC 429 compatible). ARINC 429 A data input to receiver 1.
DI1(B)	Data In 1, LO (input, ARINC 429 compatible). ARINC 429 B data input to receiver 1.
DI2(A)	Data In 2, HI (input, ARINC 429 compatible). ARINC 429 A data input to receiver 2.
DI2(B)	Data In 2, LO (input, ARINC 429 compatible). ARINC 429 B data input to receiver 2.
$\overline{DR1}$	Data ready, Receiver 1 (output, active Low). A logic 0 indicates valid data available in receiver 1
$\overline{DR2}$	Data ready, Receiver 2 (output, active Low). A logic 0 indicates valid data available in receiver 2
SEL	Receiver data select (input). Selects receiver word 1 or 2 to be read on to the data bus. Logic 0 selects receiver word 1
$\overline{OE1}$	Receiver 1 data enable (input, active Low). Logic 0 enables selected data from receiver 1 on to data bus.
$\overline{OE2}$	Receiver 2 data enable (input, active Low). Logic 0 enables selected data from receiver 2 on to data bus.
DO-D15	16-Bit Data Bus (bidirectional, Tri-state). Bidirectional data bus for reading data from either of the receivers, or for writing data into the transmitter memory or control register.
$\overline{LD1}$	Load Tx word 1 (input, active Low). Logic 0 pulse loads word 1 into the transmitter memory from data bus.
$\overline{LD2}$	Load Tx word 2 (input, active Low). Logic 0 pulse loads word 2 into the transmitter memory from data bus.
TXR	Transmitter ready (output, active High). Logic 1 indicates the transmitter memory is empty and ready to accept new data.
DO(A)	Transmitter data, HI (output. active High, return to zero). Logic 1 indicates transmitter data bit is a 1. The signal returns to zero for second half of bit time.
DO(B)	Transmitter data. LO (output, active High, return to zero). Logic 1 indicates transmitter data bit is a 0. The signal returns to zero for second half of bit time.
ENTX	Enable Transmitter, (input, active High). Logic 1 enables transmitter to send data from transmitter memory. This must be Logic 0 while writing data into transmitter memory. Transmitter memory is cleared by high-to-low transition.
$\overline{LDCW}$	Load control register, (input, active Low). Logic 0 pulse loads control register from the data bus.
NC	No connect.
1MCK	External clock, (input, TTL compatible). Master clock used by both the receivers and transmitter. The 1MHZ rate is a X10 clock for the HI data rate (100 kbps), and an X80 clock for the LO data rate (12.5 kbps)
TXCK	Transmitter clock (output). Delivers a clock frequency equal to the transmit data rate. The clock is always enabled and in phase with the data. The clock is a logic 1 during the first half of the data bit time.
$\overline{MR}$	Master Reset (input, active Low pulse). Logic 0 resets transmitter memory, bit counters, word counter, gap timers, DRn, and TXR. Used on power up and system reset. This does not affect the control register.

TABLE 4. CONTROL REGISTER FORMAT	
BIT	**DESCRIPTION**
15 (MSB)	WLSEL
14	RCYSEL
13	TXSEL
12	PARCK
11	Y2
10	X2
09	SDEN2
08	Y1
07	X1
06	SDEN1
05	$\overline{\text{SLFTST}}$
04	PAREN
03	NOT USED
02	NOT USED
01	NOT USED
00	NOT USED

$\overline{\text{DBCEN}}$ Data bit control enable (input, active Low with internal pull up to Vcc). Logic 0 enables the transmitter parity bit control function as defined by control register bit 4, PAREN. Logic 1 forces transmitter parity bit insertion regardless of PAREN value. Pin is normally left open or tied to GND.

FUNCTIONAL DESCRIPTION

CONTROL REGISTER: The DD-03282 supports a variety of options. These options are selected by data written into the control register. Data is written into the control register from the data bus when the $\overline{\text{LDCW}}$ signal is pulsed to a logic 0.

The twelve control bits are defined below and shown above in TABLE 4.

NAME DESCRIPTION

PAREN Transmitter Parity Enable (Bit 4). Enables parity bit insertion into transmitter data bit 32. Parity is always inserted if $\overline{\text{DBCEN}}$ (Pin 40) is open or HI. If $\overline{\text{DBCEN}}$ is LO, Logic 0 on PAREN inserts data on bit 32, and Logic 1 on PAREN inserts parity on bit 32.

$\overline{\text{SLFTST}}$ ① Self Test Enable (Bit 5). Logic 0 enables a wrap–around test mode which internally connects the transmitter outputs to both receiver inputs, bypassing the receiver front end. The test data is inverted before going into Receiver 2, so its data is the complement of that received by Receiver 1. The transmitter output is active during test mode.

SDEN1 ② S/D Code Check Enable RX1 (Bit 6). Logic 1 enables the Source/Destination Decoder for Receiver 1.

X1,Y1 ② S/D Compare Code RX1 (Bit 7, Bit 8). If the Receiver 1 S/D code check is enabled (SDENB1 = 1), then incoming receiver data S/D fields will be compared to Xl,Yl. If they match, the word will be accepted by Receiver 1; if not, it will be ignored. X1 (Bit 7) is compared to serial data bit 9, Y1 (Bit 8) is compared to serial data bit 10.

SDEN2 ② S/D Code Check Enable RX2 (Bit 9). Logic 1 enables the Source/Destination Decoder for Receiver 2.

X2,Y2 ② S/D Compare Code RX2 (Bit 10, Bit 11). If the Receiver 2 S/D code check is enabled (SDENB2 = 1), then incoming receiver data S/D fields will be compared to X2,Y2. If they match, the word will be accepted by Receiver 2; if not, it will be ignored. X2 (Bit 10) is compared to serial data bit 9, Y2 (Bit 11) is compared to serial data bit 10.

PARCK Parity Check Enable (Bit 12). Logic 1 inverts the transmitter parity bit. Logic 0 selects normal odd parity; logic 1 selects even parity.

TXSEL③ Transmitter Data Rate Select (Bit 13). Logic 0 sets the transmitter to the HI data rate. HI rate is equal to the clock rate divided by 10 (100 kbps for 1 MHz clock). Logic 1 sets the transmitter to the LO data rate. LO rate is equal to the clock rate divided by 80 (12.5 kbps for 1 MHz clock).

RCVSEL④ Receiver Data Rate Select (Bit 14). Logic 0 sets both receivers to accept the HI data rate. The nominal HI data rate is the input clock divided by 10 (100 kbps for 1 MHz clock). Logic 1 sets both receivers to accept the LO data rate. The nominal LO data rate is the input clock divided by 80 (12.5 kbps for 1 MHz clock).

WLSEL⑤ Word Length Select (Bit 15). Logic 0 sets the transmitter and receivers to a 32-bit word format. Logic 1 sets them to a 25-bit word format.

NOT USED When writing to the control register, the four "not used" bits are "don't care" bits. These four bits will not be used on the chip.

NOTES:

① The test mode should always conclude with ten nulls. This step prevents both receivers from accepting any invalid data stream.

② SDENBn, Xn and Yn should be changed within 20 bit times after ~~DRn~~ goes low and after the bit stream has been read, or within 30-bit times after a master reset has been removed.

③ TXSEL should only be changed during the time that TXR is high or Master Reset is low.

④ RCVSEL should be changed only during a Master Reset pulse. If changed at any other time, then the next bit stream from both Receiver 1 and Receiver 2 should be ignored.

⑤ If the control word (which includes WLSEL) is set during Master Reset, the Receiver/Transmitter operation will be correct. If the control word is changed other than during Master Reset, then TXR must be TRUE to ensure correct operation of the transmitter, and the first data stream received, in each receiver, should be ignored.

DATA FORMAT

The ARINC serial data is shuffled and formatted into two 16-bit words (WORD 1 and WORD 2) used by the bidirectional data bus interface. FIGURE 3 describes the mapping between the 32-bit ARINC serial data and the two data words. FIGURE 4 describes the mapping for the 25-bit serial word as used when control register bit WLSEL is set to logic 1.

RECEIVER OPERATION

Since the two receivers are functionally identical, only one will be discussed in detail. Each receiver consists of the following circuits:

LINE RECEIVER: The Line Receiver functions as a voltage level translator. It transforms the ±10 volt differential ARINC data signals into 5 volt internal logic levels. The line receiver is protected against shorts to ±29 volts and provides common mode voltage rejection. The outputs of the Line Receiver are one of two inputs to the Self-Test Data Selector. The other input to the Data Selector is the self-test signal from the transmitter section. The self-test signals are inverted going into Receiver 2. The data selector is controlled by Control Register bit 05 (SLFTST).

INCOMING DATA: The incoming data (either self test or ARINC) is triple sampled by the word gap timer to generate a data clock. The start of each bit is first detected and then verified two receive-clock cycles later. The receive clock is 1 MHz for HI speed and 125 kHz for LO speed operation and is generated by the Receiver/Transmitter timing circuit. The receive clock is ten times the normal data rate to ensure no data ambiguity.

DATA CLOCK: The derived data clock then shifts the data down a 32 bit long Data Shift register. The data word length is selectable for either 25 bits or 32 bits long by the Control Register bit "WLSEL." As soon as the data word is completely received, an internal signal is generated by the word-gap timer circuit to enable loading data into the 32-bit Rx buffer latch.

S/D DECODER: The Source/Destination decoder compares the user set code (X and Y) with bits 9 and 10 of the data word. (The decoder can be enabled and disabled by the "SDENB" bit of the control register). If the two codes are matched, a signal is generated to latch in the received data into the receiver buffer. Otherwise, the data word is ignored and not latched into the buffer. If the data is latched, the Data Ready output signal is set to a logic 1 to indicate to the user that a valid data word has been received and is ready to be read.

PARITY: The parity of the incoming message is checked when it is received. A logic 0 in bit 8 of word 1 indicates the received word has an odd number of 1's (no error). Logic 1 indicates the received word has an even number of 1's (error condition).

DATA ACCESS: To access the receiver data, the user sets the receiver data select line (SEL) to a logic 0 and pulses the output enable (OEn) line with a logic 0. This causes Data Word 1 to be placed on the data bus. To obtain Data Word 2, the user sets the SEL line to a logic 1 and pulses OEn with another Low. When both Word 1 and Word 2 have been read, Data Ready (DRn) will be reset. This reset is triggered by the leading edge of the final OEn.

If a new data word is received before the previous data has been read from the receiver buffer (as indicated by the DR signal flip flop), the receiver buffer will not be overwritten by the new data. (Reference Application Note AN/A-5.)

DATA ERROR CONDITIONS: If the receiver input data word string is broken before the entire data word is received, the receiver will reset and ignore the partially received data word.

If the receiver input data word string is not properly framed with at least 1 null bit before the word and 1 null bit after the word, the receiver will reset and ignore the improperly framed data word.

TRANSMITTER OPERATION

The transmitter section consists of an 8 word x 32 bit FIFO, parity generator, transmitter word-gap timer, and TTL output circuit.

FIFO BUFFER: The 8 x 32 buffer memory allows the user to load up to eight words into the transmitter, enable it, and then ignore it while the transmitter sends the data. Data is loaded into the buffer by pulsing $\overline{LD1}$ to load the first 16 bits (WORD 1) from the data bus and pulsing $\overline{LD2}$ to load WORD 2. $\overline{LD1}$ must always precede $\overline{LD2}$ for each 32-bit word. The transmitter must always be disabled while loading the buffer (ENTX = logic 0).

If the buffer is full and new data is inadvertently strobed with $\overline{LD1}$ and $\overline{LD2}$, the last 32-bit word in the buffer will be overwritten. Data will remain in the buffer until ENTX goes to a logic 1, which will cause data to be shifted out serially.

The buffer data is transmitted until the last word in the buffer is shifted out. At this time a transmitter ready signal (TXR) is set to a logic 1 indicating that the buffer is empty and ready to receive up to eight more data words. Writing into the buffer memory is disabled when ENTX is set to logic 1.

READY SIGNAL: The transmitter ready signal (TXR) is set to logic 0 with the first occurrence of a $\overline{LD2}$ pulse to indicate that the buffer is not empty.

OUTPUT REGISTER: The output register can shift out a word of 32 or 25 bits as controlled by control register bit "WLSEL."

TX WORD GAP: The TX word gap timer circuit inserts a 4-bit timer gap between words. This gives a minimum requirement of a 36-bit time (or 29-bit time in the 25-bit mode) for each word transmission. The 4-bit time gap is also automatically maintained when a new block of data is loaded into the buffer, which may take less than interword gap time.

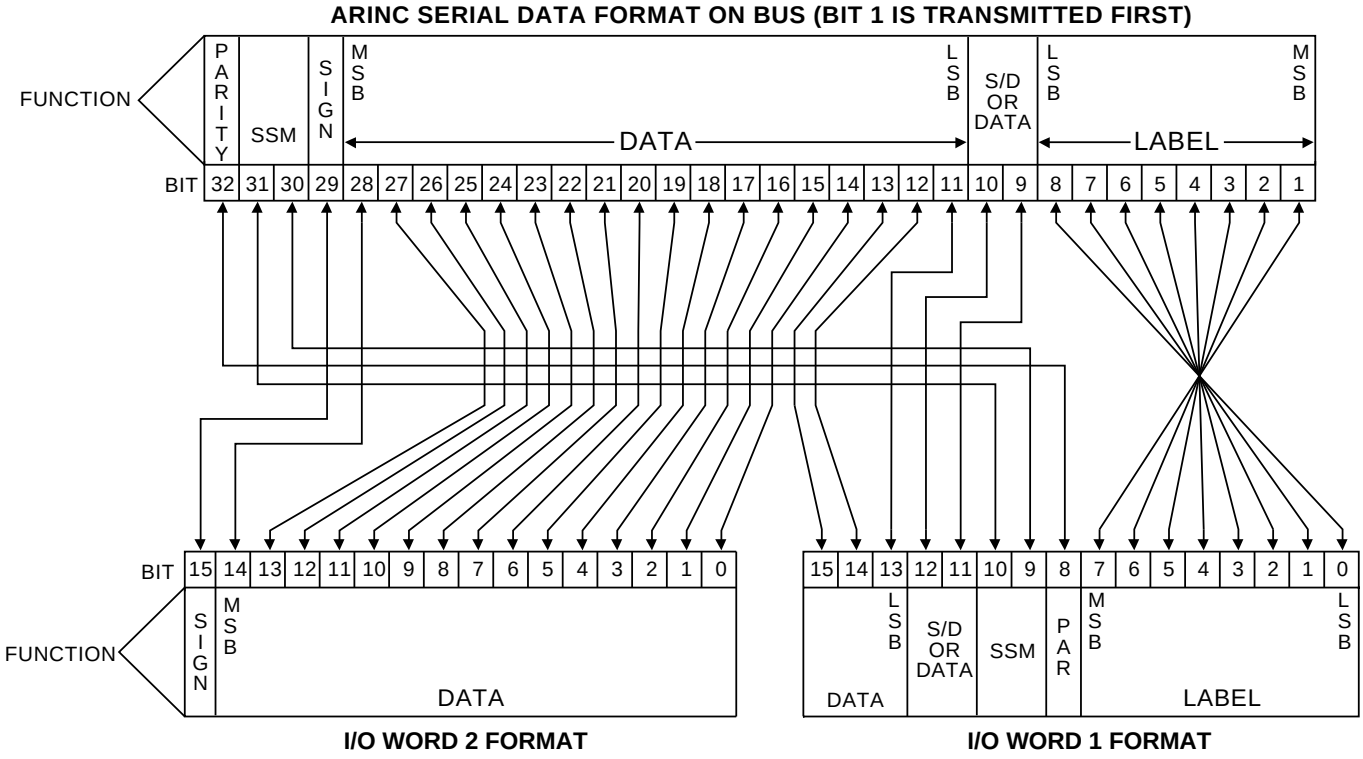


FIGURE 3. MAPPING OF SERIAL DATA TO/FROM WORD 1 AND WORD 2 — 32-BIT FORMAT

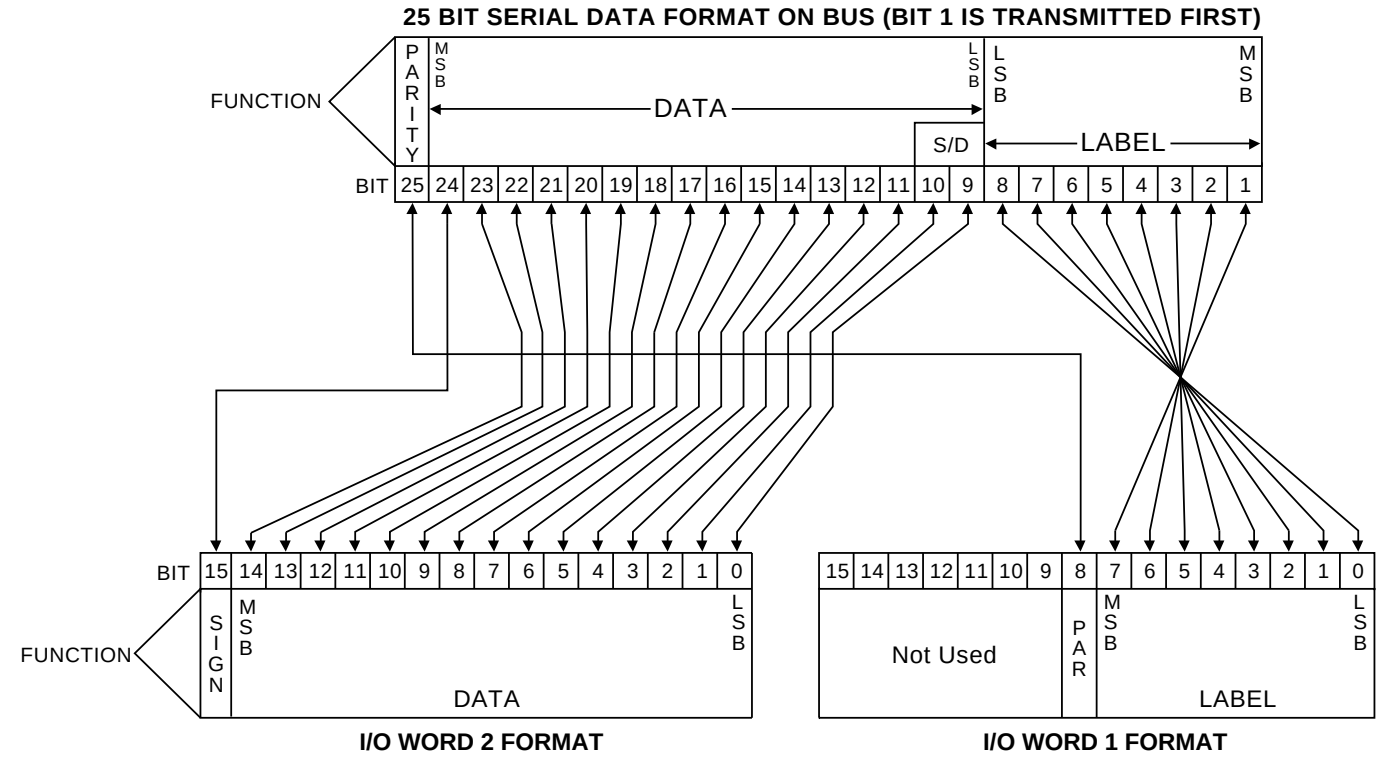


FIGURE 4. MAPPING OF SERIAL DATA TO/FROM WORD 1 AND WORD 2 — 25-BIT FORMAT

PARITY GENERATOR: The parity generator calculates either odd or even parity as specified by control register bit "PARCK." Odd parity is normally used; even parity is available to test the receive parity check circuit. Bit 8 of word one is replaced with a parity bit during serial transmission if parity is selected by the control register bit "PAREN" and the $\overline{\text{DBCEN}}$ pin. Otherwise, bit 8 is passed through as data.

TRANSMITTER OUTPUT: The transmitter outputs TTL compatible signals: DO(A) and DO(B). DO(A) and DO(B) are the transmitter data in two rail, return-to-zero format. DO(A) indicates a logic 1 data bit by going to a 1 for the first half of a bit time, then returning to 0 for the second half; DO(B) remains at 0 for the whole bit time.

In the same fashion, DO(B) indicates a logic 0 data bit by pulsing HI while DO(A) remains LO. A null bit is indicated when both signals remain LO. It is illegal for both signals to be logic 1.

The TXCLK is a continuous clock signal of 50% duty cycle synchronous with transmitter data. The clock will always be logic 1 during the first half of a bit time.

POWER-UP RESET:

An internal power-up reset circuit prevents erroneous data transmission before an external master reset has been applied.

25-BIT WORD OPERATION

The Transceiver implements a 25-blt word format which may be used in non-ARINC applications to enhance data transfer rate.

The format is a simplified version of the 32-bit ARINC word and is illustrated in FIGURE 4. It consists of an 8-bit label, a 16-bit data word, and a parity bit. The parity bit can optionally be replaced with a 17th data bit. The Source/Destination code checking option can be enabled in either receiver. It will operate on bits 9 and 10 of the 25-bit word.

SELF-TEST OPERATION

By clearing the control register bit ($\overline{\text{SLFTST}}$) self-test option, the user may perform a functional test of the Transceiver. The user can write data into the transmitter and it will be internally wrapped around into both receivers. The user can then verify reception and integrity of the data. (Self-test data input to channel 2 is inverted.) The ARINC 429 line receiver interface and the external line drivers are not tested.

By setting the transmitter to use even parity, the user can test the receiver's parity circuit operation.

POWER-UP RESET AND MASTER RESET

The user must apply a logic 0 pulse to the Master Reset pin ($\overline{\text{MR}}$) after power up or upon system reset. Preceding the master reset at power-up an internal power-up reset occurs which will clear the transmitter so that no erroneous data will be transmitted before master reset. Receivers and the internal control logic are reset by Master Reset.

In order to guarantee correct reception of the very first ARINC 429 words after a power-on sequence, the user should issue the Master Reset pulse after the control register is programmed. The Master Reset has no effect on the data loaded in the Control Register. (Reference Application Note AN/A-5.)

FIGURE 5 shows a typical reset and initialization sequence. The user must pulse the $\overline{\text{MR}}$ pin low to reset the device. To load the Control Register from the data bus, the $\overline{\text{LDCW}}$ pin is pulsed low while the desired control data is applied on the data bus.

PROCESSOR INTERFACE

FIGURE 6 shows a typical read/write timing sequence and FIGURE 7 shows a typical transmitter loading sequence.

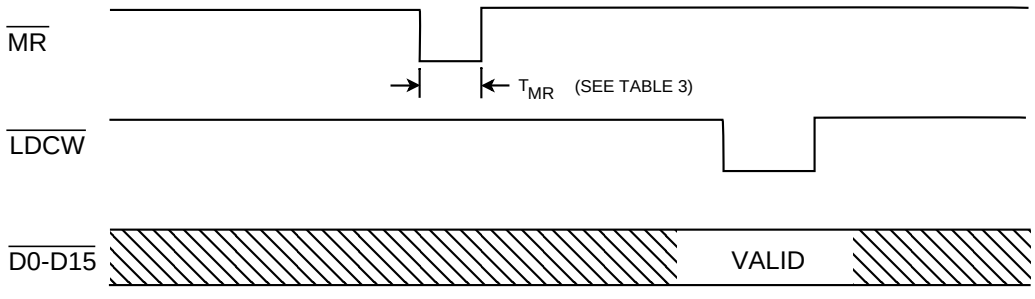


FIGURE 5. RESET AND INITIALIZATION SEQUENCE

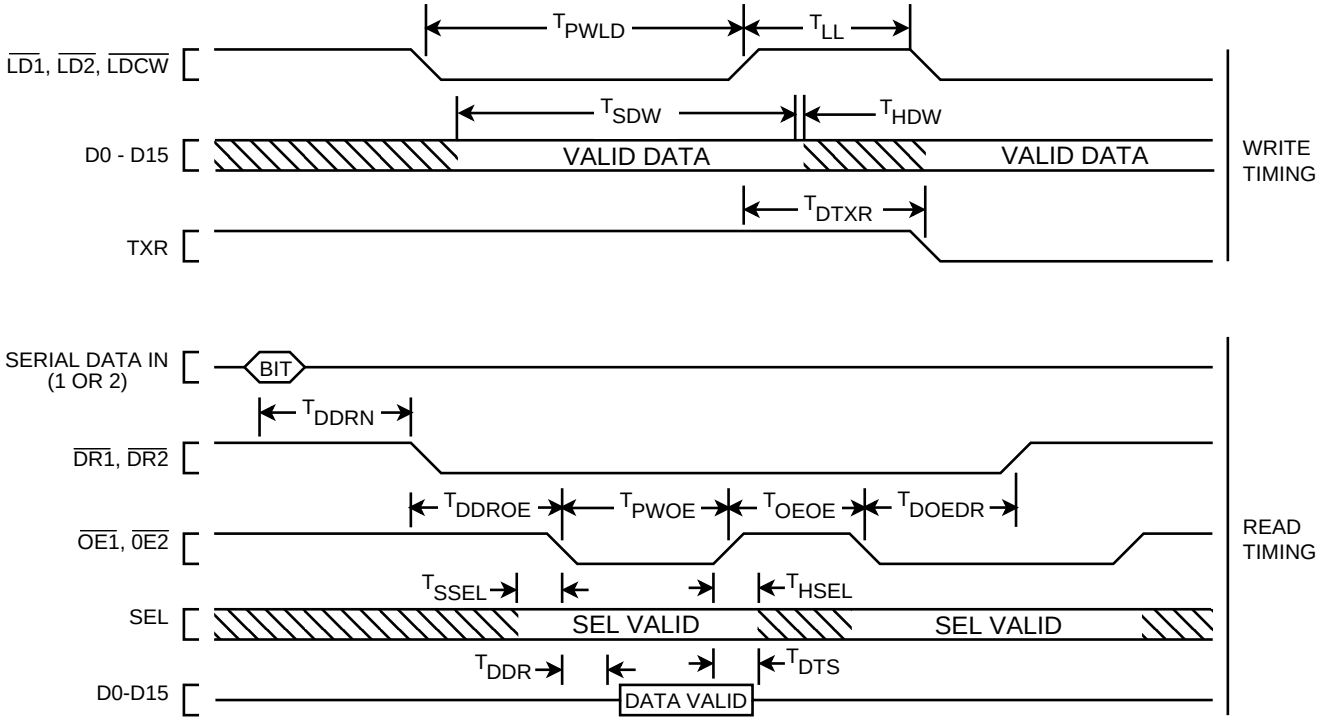


FIGURE 6. READ/WRITE TIMING

TABLE 5. DD-03282 READ/WRITE SPECIFICATION

SYMBOL	PARAMETER	DATA RATE 100 kb/s MIN	DATA RATE 100 kb/s MAX	DATA RATE 12.5 kb/s MIN	DATA RATE 12.5 kb/s MAX	UNITS
	WRITE CYCLE TIMING					
T_{PWLD}	$\overline{LD1}$, $\overline{LD2}$ and $\overline{LDCW}$ Pulse Width	130			130	ns
T_{LL}	Delay Between Consecutive Load Pulse from LD1 to LD2	0		0		ns
T_{SDW}	Data to $\overline{LD}\uparrow$ Set-Up Time	110		110		ns
T_{HDW}	Data to $\overline{LD}\uparrow$ Hold Time	15		15		ns
T_{DTXR}	Delay $\overline{LD2}\uparrow$ to TXR$\downarrow$		840		840	ns
	READ CYCLE TIMING					
T_{DDRN}	Delay, Bit 32/25 in$\uparrow$ to $\overline{DRn}\downarrow$		18		144	µs
T_{DDROE} T_{PWOE}	Delay, $\overline{DRn}\downarrow$ to $\overline{OEn}\downarrow$, $\overline{OE1}$ or $\overline{OE2}$ pulse width	0 200		0 200		ns
T_{OEOE}	Delay Between Consecutive $\overline{OE}$ Pulses	50		50		ns
T_{DOEDR}	Delay, 2nd $\overline{OE}\uparrow$ to $\overline{DRn}$ Reset ($\uparrow$)		200		200	ns
T_{SSEL}	SEL to $\overline{OE}\downarrow$ to Valid Data	20		20		ns
T_{HSEL}	SEL to $\overline{OE}\uparrow$ Hold Time	20		20		ns
T_{DDR}	Delay $\overline{OE}\downarrow$ to Valid Data		200		200	ns
T_{DTS}	Delay $\overline{OE}\uparrow$ to Data Hi-Z	10	50	10	50	ns

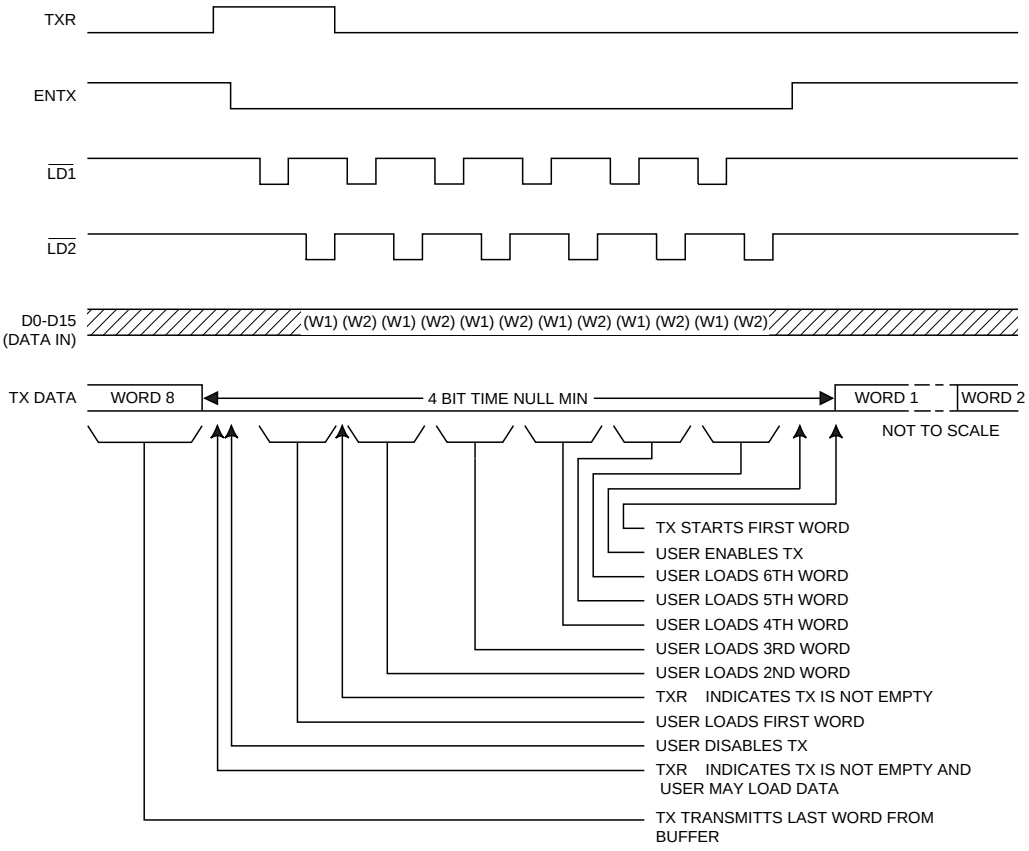


FIGURE 7. TYPICAL TRANSMITTER LOAD SEQUENCE

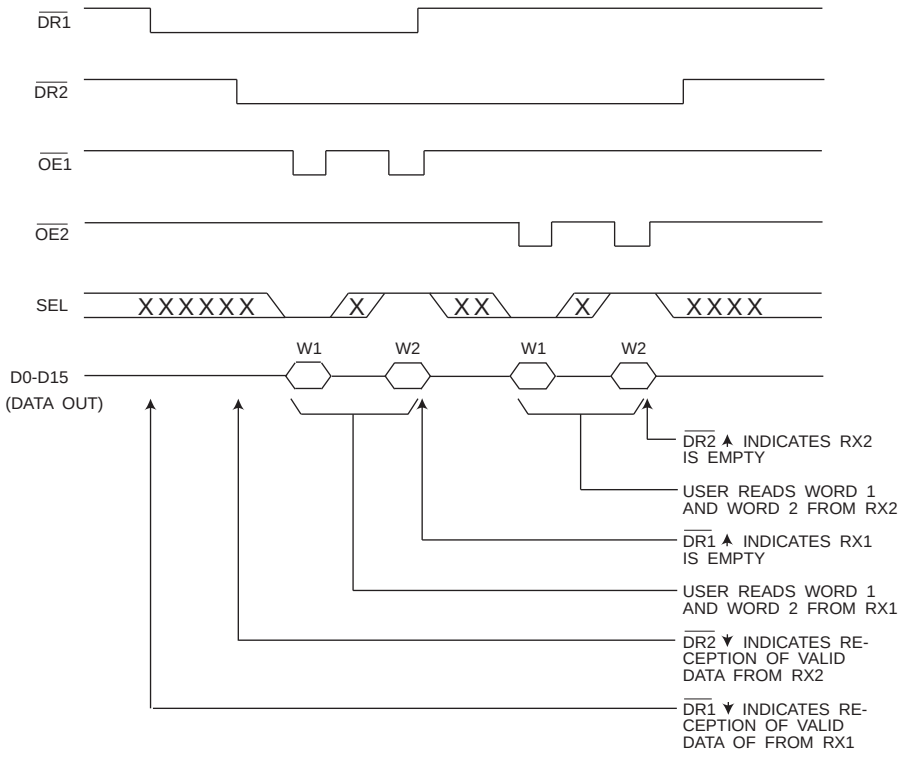


FIGURE 8. TYPICAL RECEIVER READ SEQUENCE

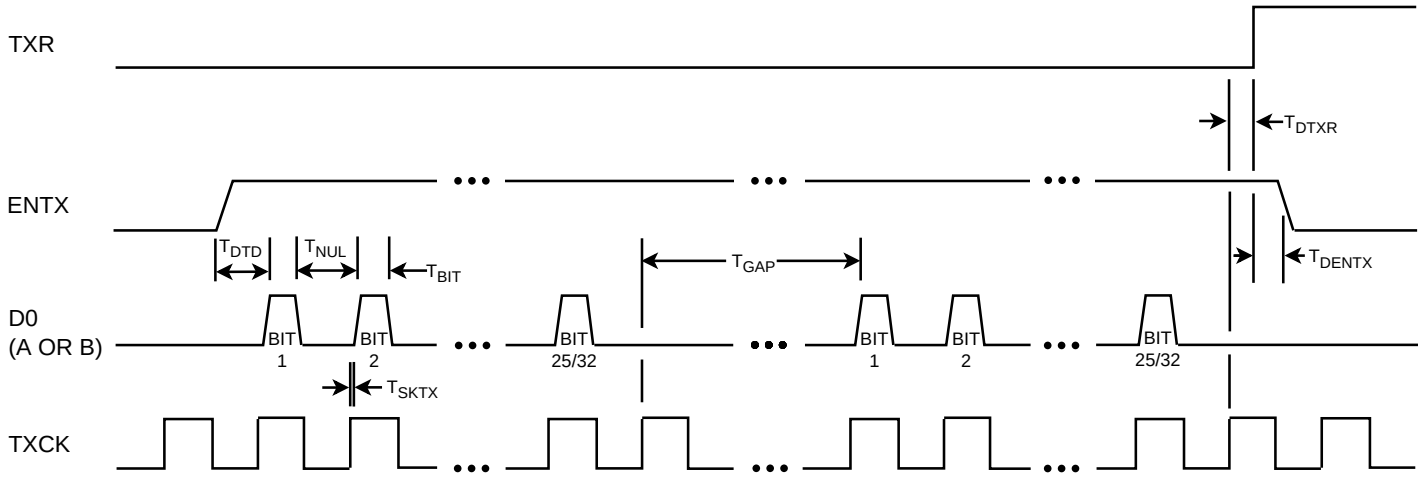


FIGURE 9. TRANSMITTER TIMING

TABLE 6. DD-03282 TRANSMITTER TIMING SPECIFICATION

SYMBOL	PARAMETER	DATA RATE 100 kb/s		DATA RATE 12.5 kb/s		UNITS
		MIN	MAX	MIN	MAX	
T_{DTD}	Delay, ENTX↑ to output data*		25		200	µs
T_{NUL}	Output data null time	4.95	5.05	39.6	40.4	µs
T_{BIT}	Output data bit time	4.95	5.05	39.6	40.4	µs
T_{SKTX}	Data skew between TXCK↑(↓) and D0↑ (↓)	0	±50	0	±50	ns
T_{GAP}	Data word gap time	39.6	40.4	316.8	323.2	µs
T_{DTXR}	Delay, end of TX word to TXR↑		50		50	ns
T_{DENTX}	Delay, TXR↑ to ENTX↓	0		0		ns

*This applies only when there has been a 4-bit null since the end of the transmitted data.

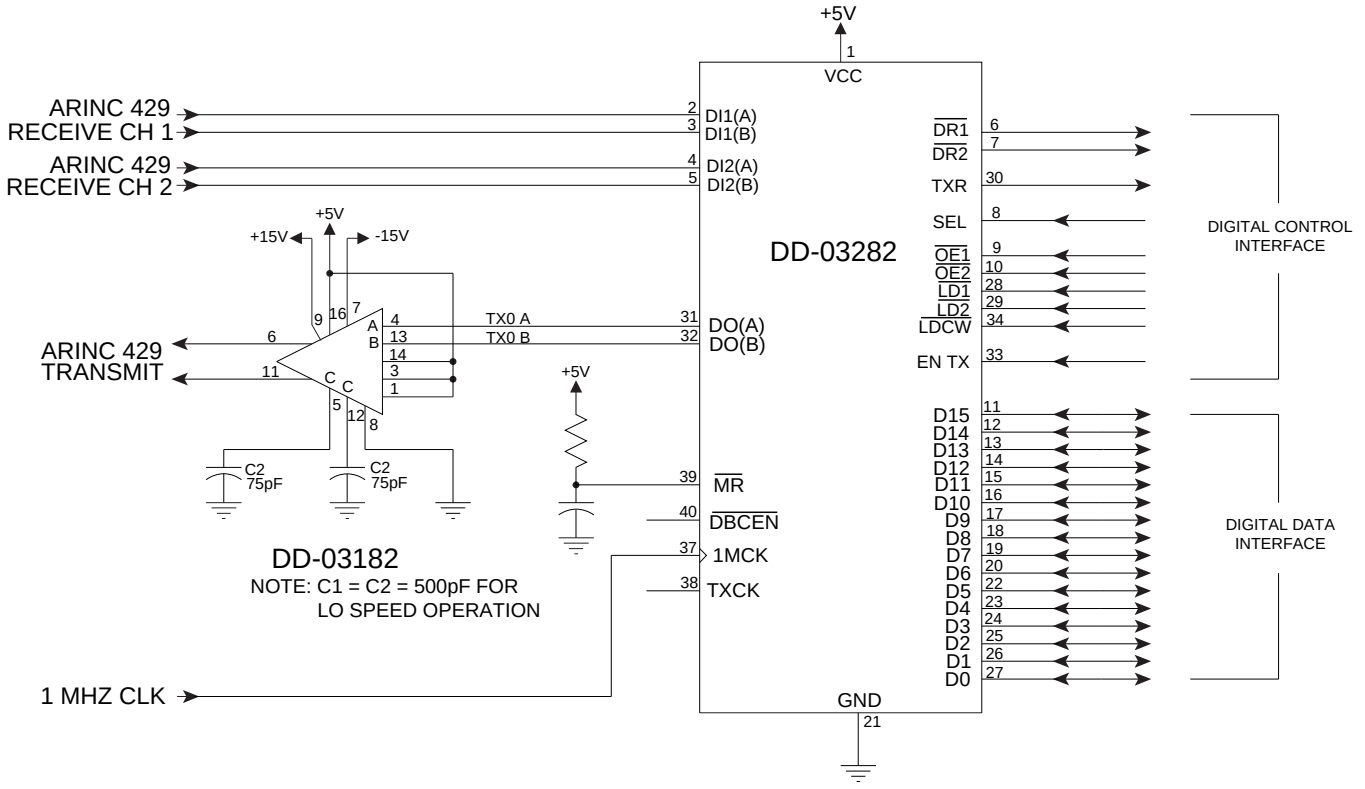


FIGURE 10. TYPICAL TRANSCEIVER/LINE DRIVER INTERCONNECT CONFIGURATION

As shown in FIGURE 7 a typical sequence begins with the transmitter completing a logic 1 transmission of the previous data block. The TXR signal notifies the user that data may be loaded into the buffer. The user sets ENTX to logic 0 to disable the Transmitter and proceeds to load a total of six ARINC words into the buffer. (Note that up to eight words could have been loaded).

The user then enables the transmitter by setting ENTX to a logic 1 causing the transmitter to begin the sequence of sending out data words. Although not shown in the figure, the transmitter load sequence can be interleaved with the receiver read cycles with no interference between the two operations.

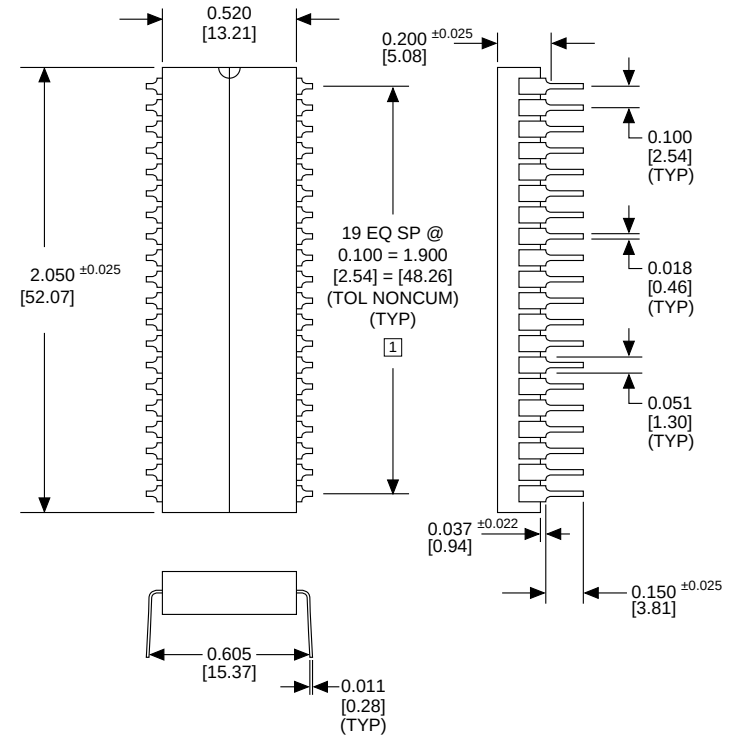
FIGURE 8 shows a typical receiver read sequence.

Both receivers notify the user that valid data has been received by setting their respective DRn lines to logic 0. The user responds by reading the two data words from Receiver 1 and/or Receiver 2.

The SEL line is normally a system address line and may assume any state, but must be valid when the OEn line is pulsed low.

TABLE 7. DD-03182 LINE DRIVER SPECIFICATIONS

PARAMETER	UNITS	MIN	TYP	MAX
ABSOLUTE MAXIMUM RATINGS				
VOLTAGE BETWEEN PINS				
• +V & -V	V			40
• V1 & GND	V			7
• V_{REF} & GND	V			6
POWER SUPPLY REQUIREMENTS				
• +V	VDC	10.5	15	16.5
• -V	VDC	-10.5	-15	-16.5
• V1	VDC	4.75	5	5.25
• V_{REF}	VDC	4.75	5	5.25
THERMAL				
Operating Temperature	°C	-55		+125
Storage Temperature	°C	-65		+150
Lead Temperature (localized 10 sec duration)	°C			+300



1 LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN +0.010

2 DIMENSIONS SHOWN ARE IN INCHES [MILLIMETERS]

FIGURE 11. DD-03282 DIP MECHANICAL OUTLINE

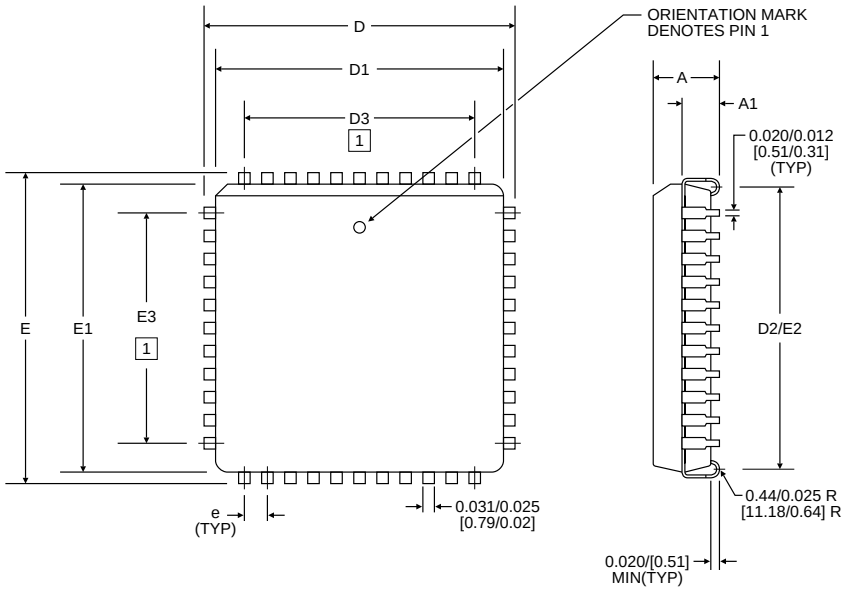
SERIAL INTERFACE

The transmitter clock (TXCK) is free running and in phase with the transmitter data. The transmitter data (DO(A) and DO(B)) are TTL levels. There are always at least 4 null bits between data words.

The receiver signals (DIn (A) and DIn (B) where n=1 or 2) are differential, bipolar, return-to-zero logic signals. FIGURE 10 is an example of how to connect the DD-03282 to the DD-03182 Line Driver. The receive data is normally asynchronous to the transmitter and can also be at a different data rate than the transmitter.

ARINC 429 LINE DRIVER

The DD-03282 requires a line driver to put ARINC 429 data on the serial data bus. DDC's DD-03182 ARINC 429 line driver will support ARINC 429, 571, and 575 standards. FIGURE 10 illustrates a typical interconnection configuration between the DD-03282 Transceiver and the DD-03182 ARINC 429 Line Driver. TABLE 7 shows the DD-03182 Line Driver Specifications. Refer to the DD-03182 data sheet for further information about the ARINC 429 Line Driver.

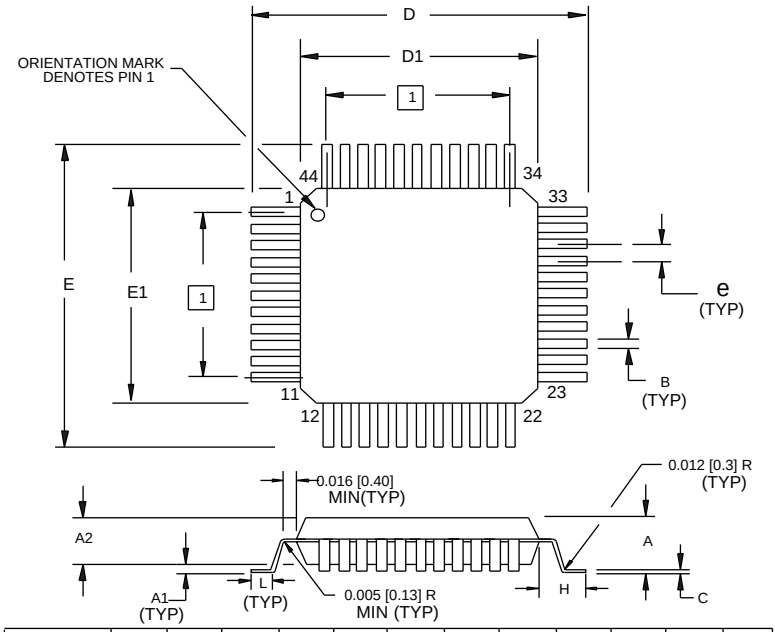


		A	A1	D1	D2	D3	E1	E1	E3	e	D	E
MIN	INCHES	0.165	0.090	0.649	0.590	0.500	0.650	0.590	0.500	0.500	0.685	0.685
MAX		0.180	0.119	0.655	0.630	0.500	0.655	0.630	0.500	0.500	0.694	0.694
MIN	MM	4.20	2.29	16.51	14.99	12.70	16.51	14.99	12.70	1.27	17.40	17.40
MAX		4.57	3.04	16.66	16.00	BSC	16.66	16.00	BSC	BSC	17.65	17.65

1 LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±0.010

2 DIMENSIONS SHOWN ARE IN INCHES [MILLIMETERS]

FIGURE 12. DD-03282 PLCC MECHANICAL OUTLINE



		A	A1	A2	D	D1	E	E1	L	e	B	H	C
MIN	INCHES	-	0.004	0.077	0.537	0.390	0.537	0.390	0.026	0.031	0.012	0.077	0.005
MAX		0.093	0.010	0.083	0.557	0.398	0.557	0.398	0.037	BSC	0.018	REF	0.009
MIN	MM	-	0.10	1.95	13.65	9.90	13.65	9.90	0.65	0.80	0.30	1.95	0.13
MAX		2.35	0.25	2.10	14.15	10.10	14.15	10.10	0.95	BSC	0.45	REF	0.23

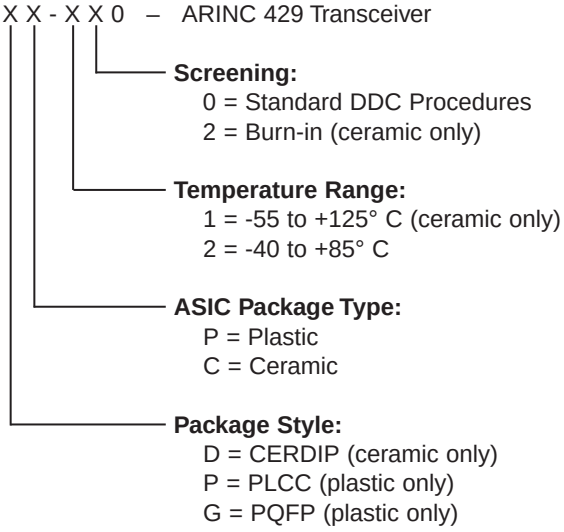
1 LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN [0.00039]

2 DIMENSIONS SHOWN ARE IN INCHES [MILLIMETERS]

FIGURE 13. DD-03282GP MECHANICAL OUTLINE

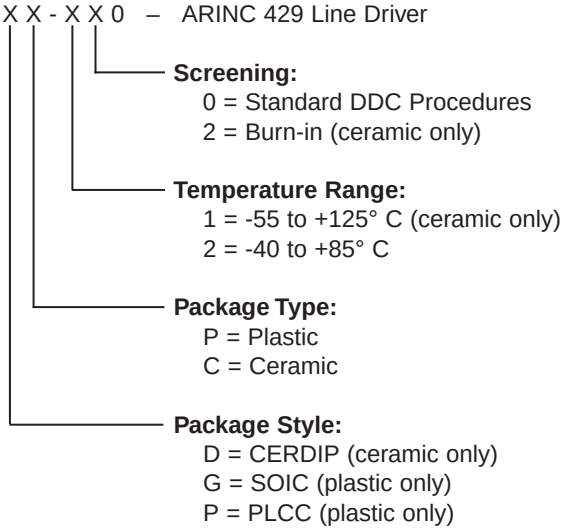
ORDERING INFORMATION

DD-03282 X X - X X 0 – ARINC 429 Transceiver



ADDITIONAL HARDWARE

DD-03182 X X - X X 0 – ARINC 429 Line Driver



For more detailed information, please refer to the DD-03182 data sheet.

OTHER APPLICABLE DOCUMENTS

ARINC Specification 429 Mark 33 Digital Information Transfer System

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