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Est. 1988

Statement of Volatility
PN: PCIe3IP & PCIe5IP

Manufacturer Part Number: PCIe3IP & PCIe5IP, includes all options (-BB, -EJ, etc.)
Manufacturer Part Description: 1 lane PCIe carrier with 3 or 5 IP Positions, local power supplies and user features.
Memory Type: FPGA and FLASH
Memory Size: FPGA Lattice LFE3-35EA: Internal registers for configuration, FIFO memory to support link traffic. FIFO on PCIe lanes includes read completion buffers..

FLASH : 4Mx16. Memory to provide power on configuration to FPGA. Not user accessible.

Volatility: FIFO memory is continuously rewritten during operation and effectively cleared by this process**.** FLASH is non-volatile.
User Accessible: FIFO within FPGA is not user accessible in the traditional sense as the PCIe traffic is flowing through these memories without user control.
Clearing Procedure: Use and Power cycle for FIFO memory. To clear the FLASH a standard 3 pass write cycle would be required.
Notes or Warnings: None